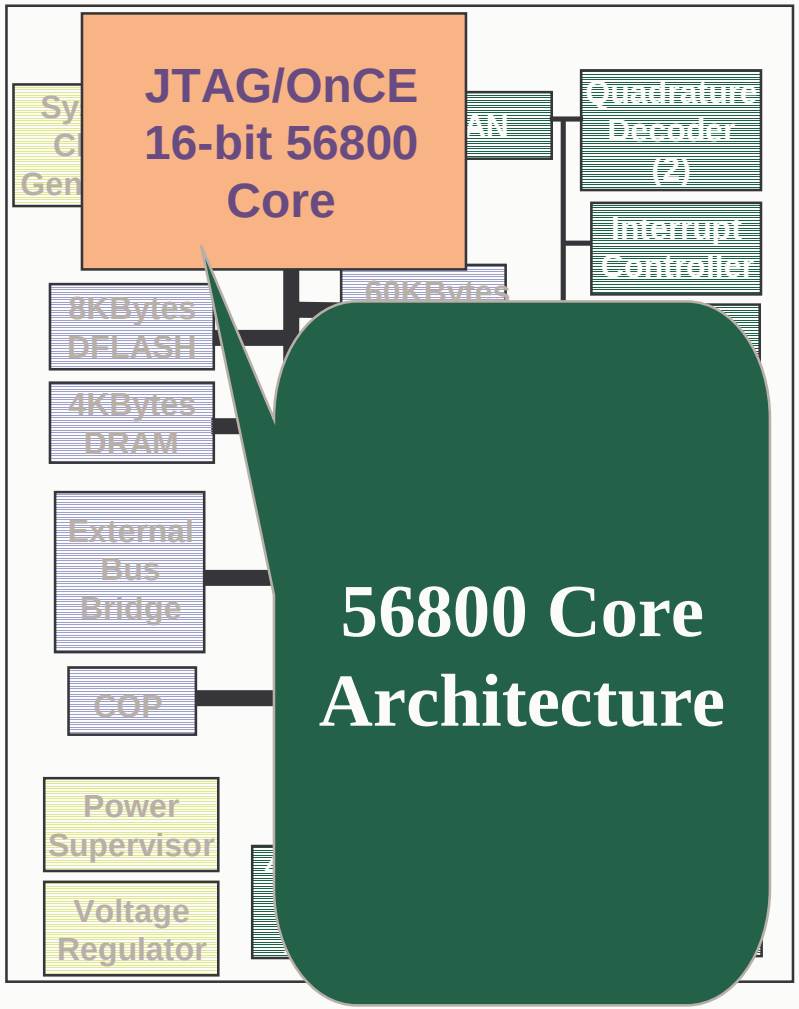
Motorola DSP56800 Solutions

Fast Flash DSP Controllers

Motorola DSP Solutions Contents

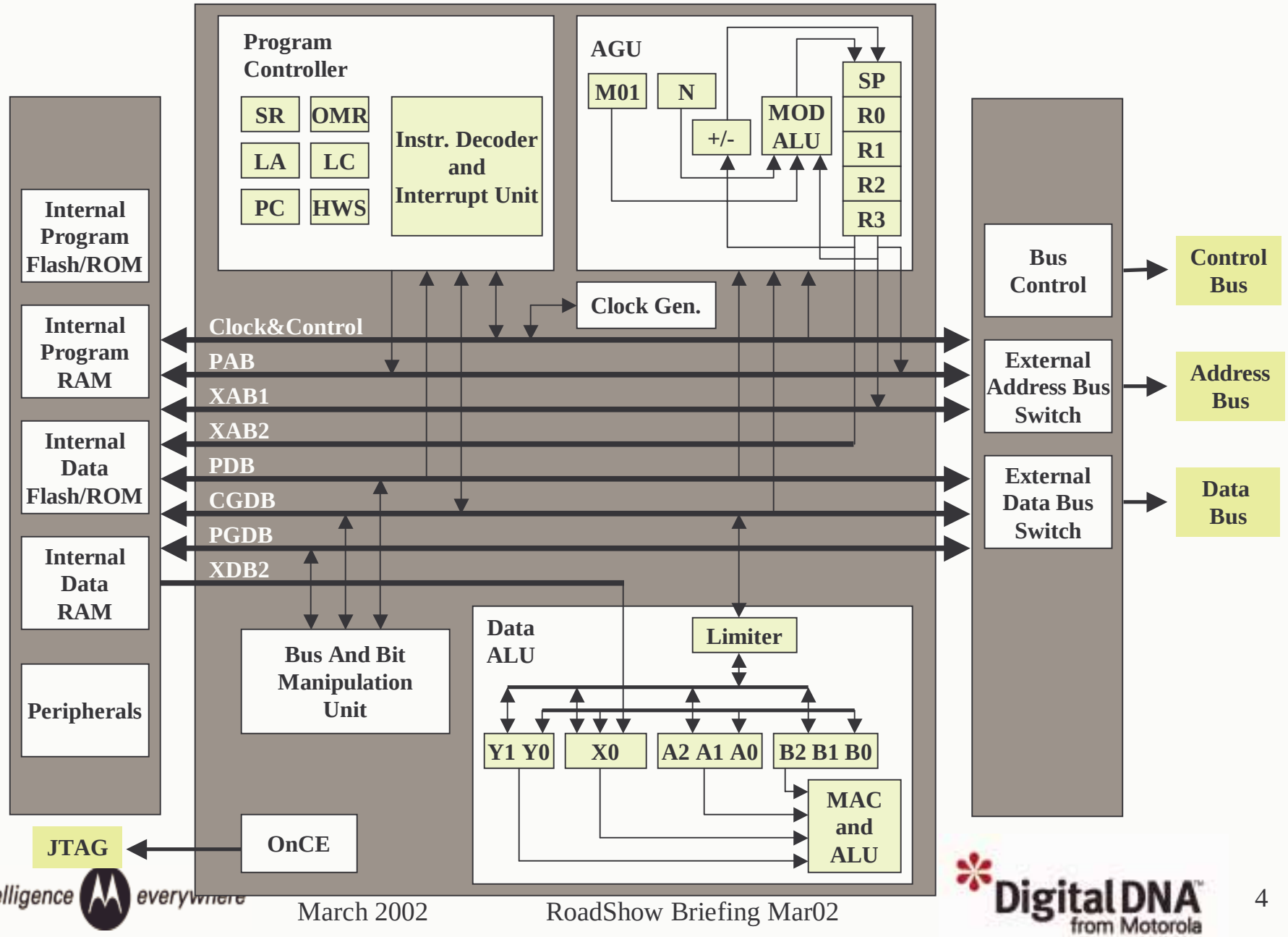
- Introduction to 56800 Architecture
- DSP56800 Peripherals
- Evaluation Module Development Systems
- Exploring Target Markets
- Development Tools
- Accessing Information

56800 Core Architecture

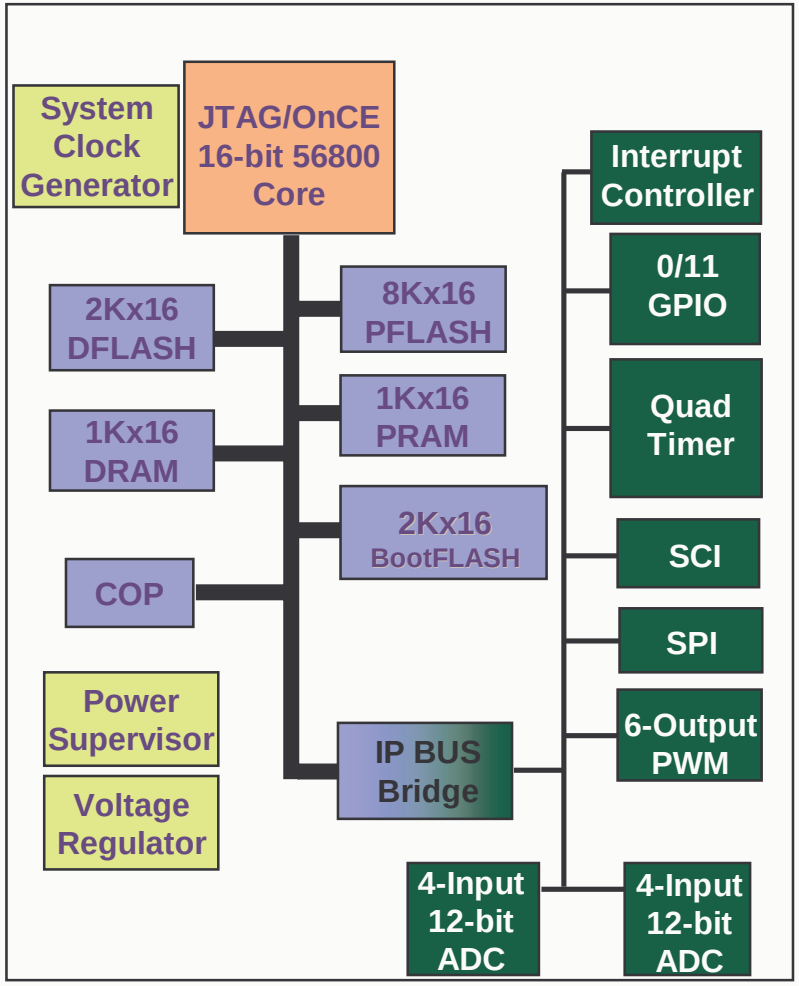


- ✓General Purpose, Register File based ALU provides optimal code density and performance
  - ✓ Any register can serve as source/destination of ALU operations
- ✓MCU Style Features for ease of programmability and enhanced compiler efficiency
  - ✓ 19 different addressing modes
  - ✓ True SW Stack supports subroutines
  - ✓ Bit manipulation
  - ✓ Flexible user-defined, multi-level interrupt priority support
- ✓OnCE™ (on-chip emulation) module allowing for debug capability throughout system design
  - ✓ Provides non-intrusive application debug
  - ✓ Full visibility to core, peripherals and memory
  - ✓ Accessible through JTAG interface
  - ✓ Enables real-time debug of application software

DSP56800 Core Block Diagram

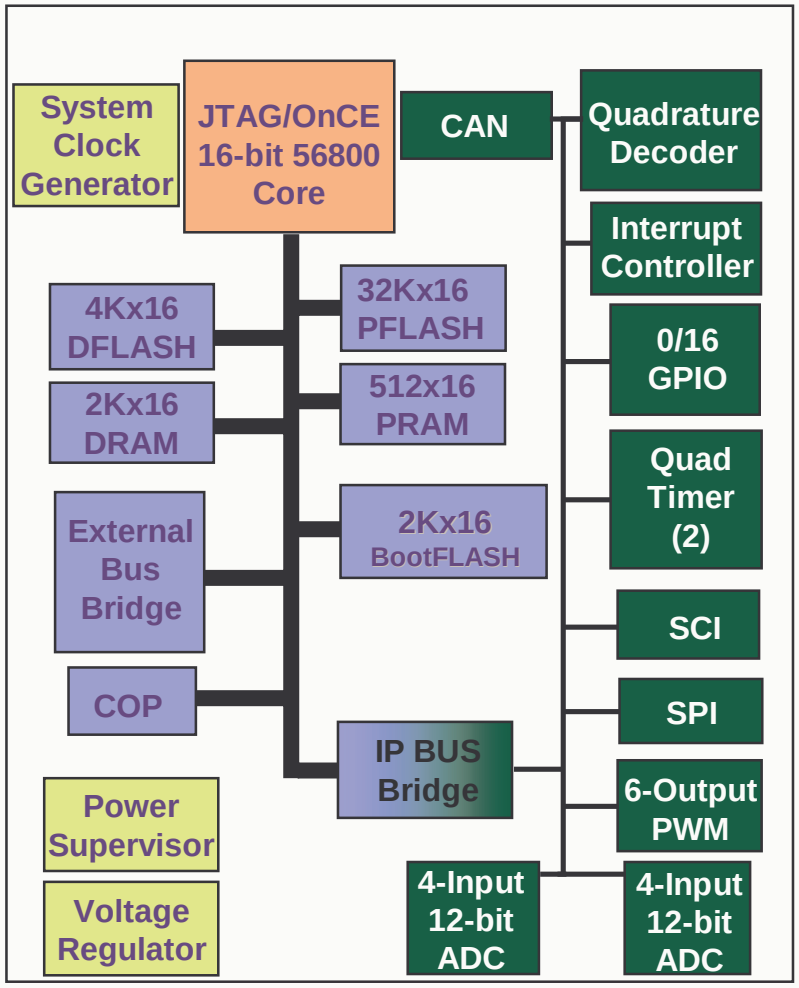


56F801 Functional Block Diagram



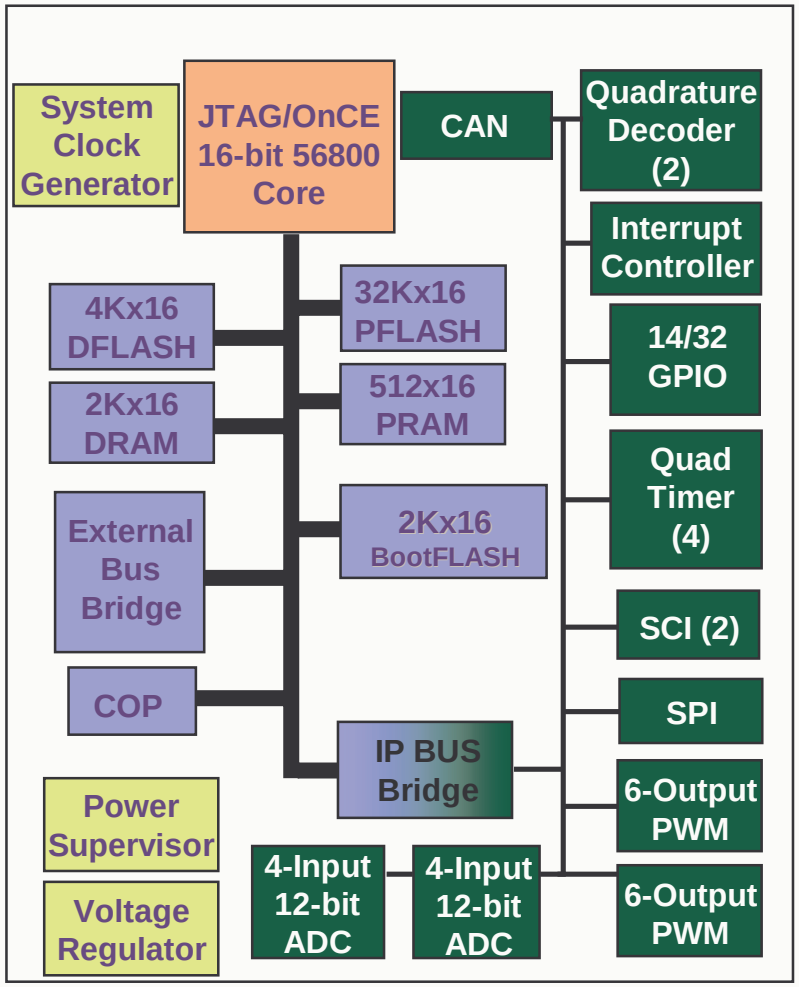
- ✓ 8Kx16 Program Flash, 1Kx16 Program RAM
- ✓ 2Kx16 Data Flash, 1Kx16 Data RAM
- ✓ 2Kx16 BootFLASH
- ✓ Voltage regulator
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ 6-Output PWM Module
- ✓ Two 4-Input 12-bit ADC
- ✓ 16-Bit Quad Timer
- ✓ COP Timer
- ✓ Multiple Serial Ports
- ✓ Up to 11 General Purpose I/OPins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE™ Debug Port

56F803 Functional Block Diagram



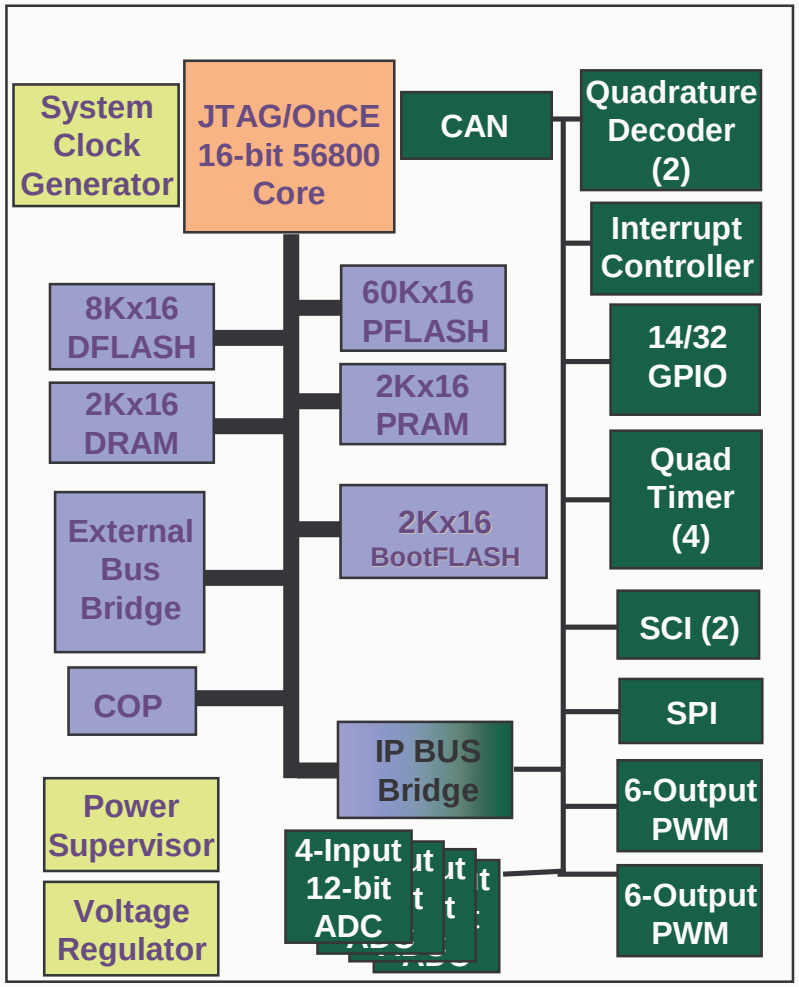
- ✓ 32Kx16 Program Flash, 512x16 Program RAM
- ✓ 4Kx16 Data Flash, 2Kx16 Data RAM
- ✓ 2Kx16 BootFLASH
- ✓ Voltage regulator
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ COP Timer
- ✓ CAN Module - 2.0B Compliant
- ✓ Quadrature Decoder
- ✓ 6-Output PWM Module
- ✓ Two 4-Input 12-bit ADC
- ✓ Two 16-Bit Quad Timers
- ✓ Multiple Serial Ports
- ✓ Up to 16 General Purpose I/O Pins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE™ Debug Port

56F805 Functional Block Diagram



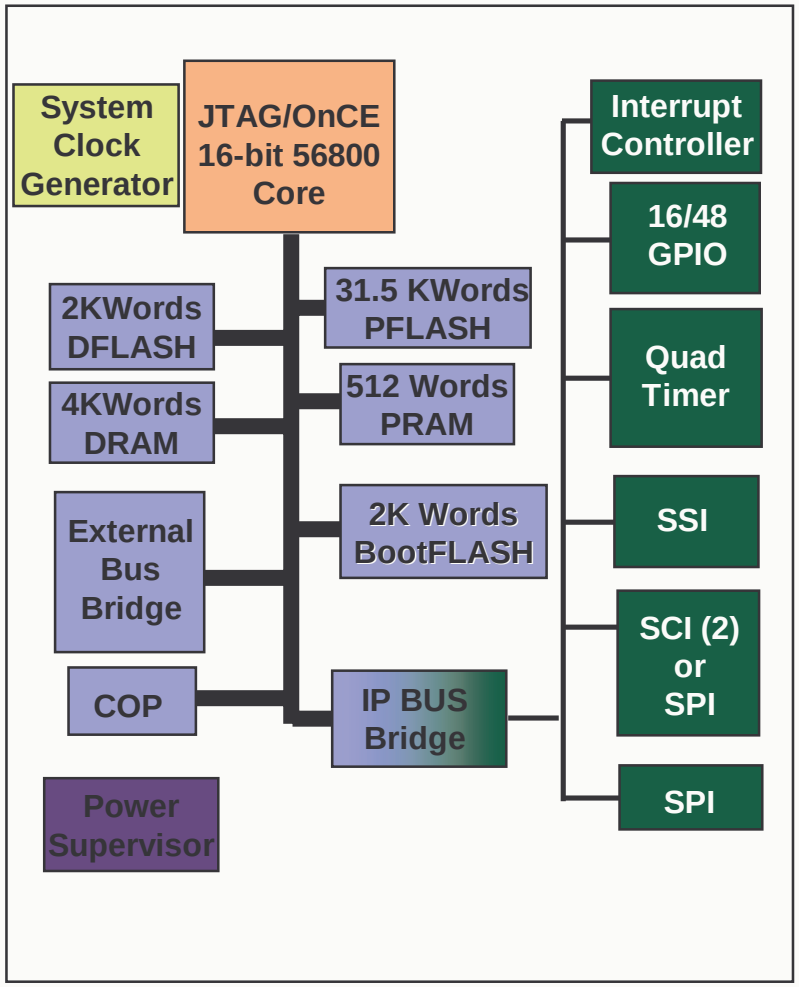
- ✓ 32Kx16 Program Flash, 512x16 Program RAM
- ✓ 4Kx16 Data Flash, 2Kx16 Data RAM
- ✓ 2Kx16 BootFLASH
- ✓ Voltage regulator
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ COP Timer
- ✓ CAN Module - 2.0B Compliant
- ✓ Two 6-Output PWM Modules
- ✓ Two Quadrature Decoders
- ✓ Two 4-Input 12-bit ADC
- ✓ Four 16-Bit Quad Timers
- ✓ Multiple Serial Ports
- ✓ Up to 32 General Purpose I/O Pins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE™ Debug Port

56F807 Functional Block Diagram



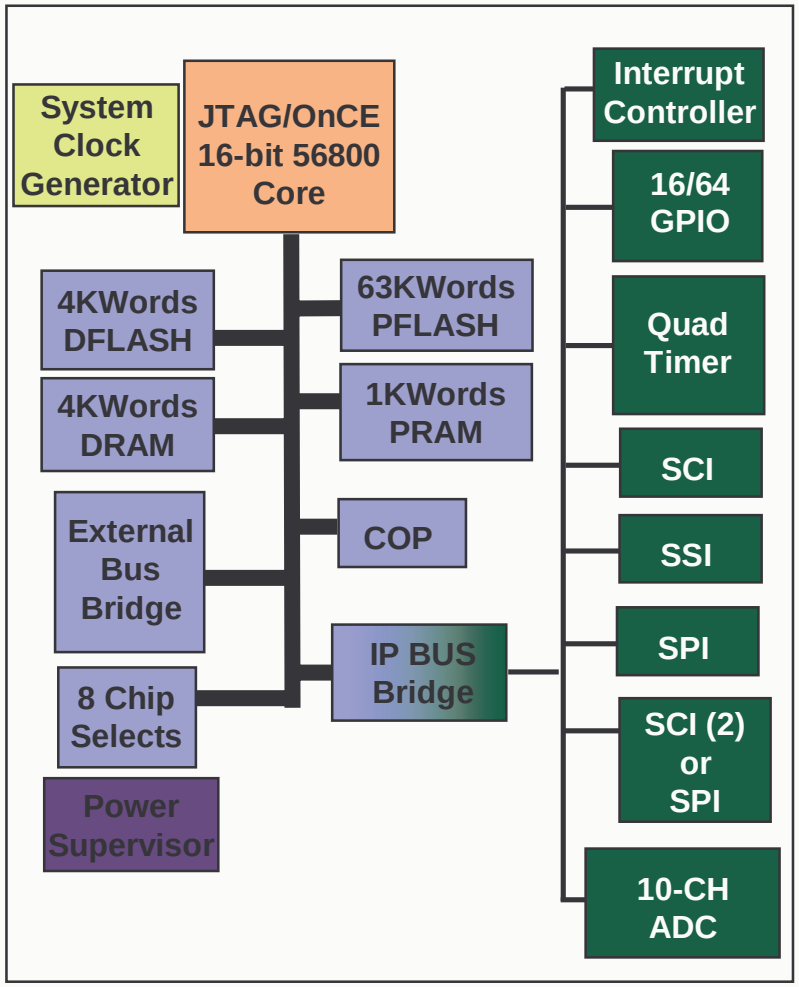
- ✓ 60Kx16 Program Flash, 2Kx16 Program RAM
- ✓ 8Kx16 Data Flash, 2Kx16 Data RAM
- ✓ 2Kx16 BootFLASH
- ✓ Voltage regulator
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ COP Timer
- ✓ CAN Module - 2.0B Compliant
- ✓ Two 6-Output PWM Modules
- ✓ Two Quadrature Decoders
- ✓ Four 4-Input 12-bit ADC
- ✓ Up to four 16-Bit Quad Timers
- ✓ Multiple Serial Ports
- ✓ Up to 32 General Purpose I/O Pins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE™ Debug Port

DSP56F826 Functional Block Diagram



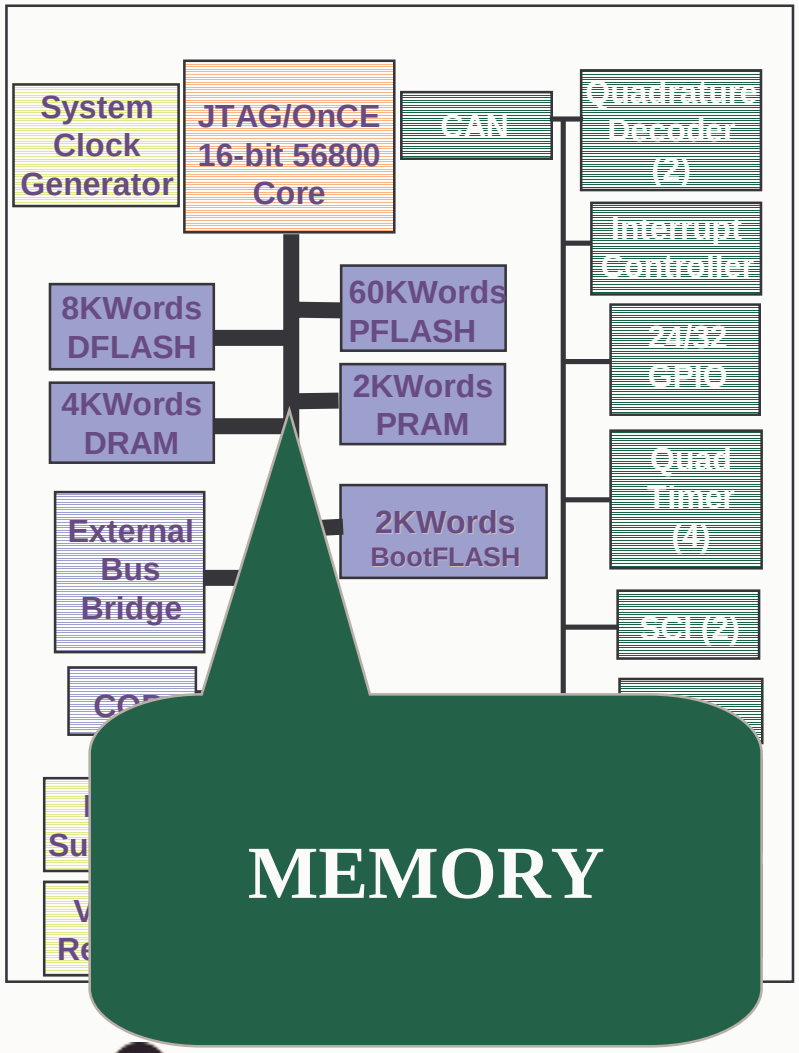
- ✓ 31.5K Words Program FLASH
  512 Words Program RAM
- ✓ 2K Words Data FLASH
  4K Words Data RAM
- ✓ 2K Words BootFLASH
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ COP/Watchdog Timer
- ✓ 16-Bit Quad Timer
- ✓ Time of Day Timer
- ✓ Multiple Serial Ports
- ✓ Up to 48 General Purpose I/O Pins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE Debug Port
- ✓ Split Voltage Supply 2.5/3.3V
- ✓ 100 LQFP Package

DSP56F827 Functional Block Diagram



- ✓ 63KWords Program FLASH, 1KWords Program RAM
- ✓ 4KWords Data FLASH, 4KWords Data RAM
- ✓ System Clock Generator
- ✓ Power Supervisor
- ✓ COP Timer
- ✓ 10-Channel, 12-bit ADC
- ✓ 16-Bit Quad Timer with DAC functionality
- ✓ Time of Day Timer
- ✓ Multiple Serial Ports
- ✓ Up to 64 General Purpose I/O Pins
- ✓ Vectored Interrupt Controller
- ✓ JTAG/OnCE Debug Port
- ✓ Split Voltage Supply 2.5/3.3V
- ✓ 128 LQFP Package

Memory

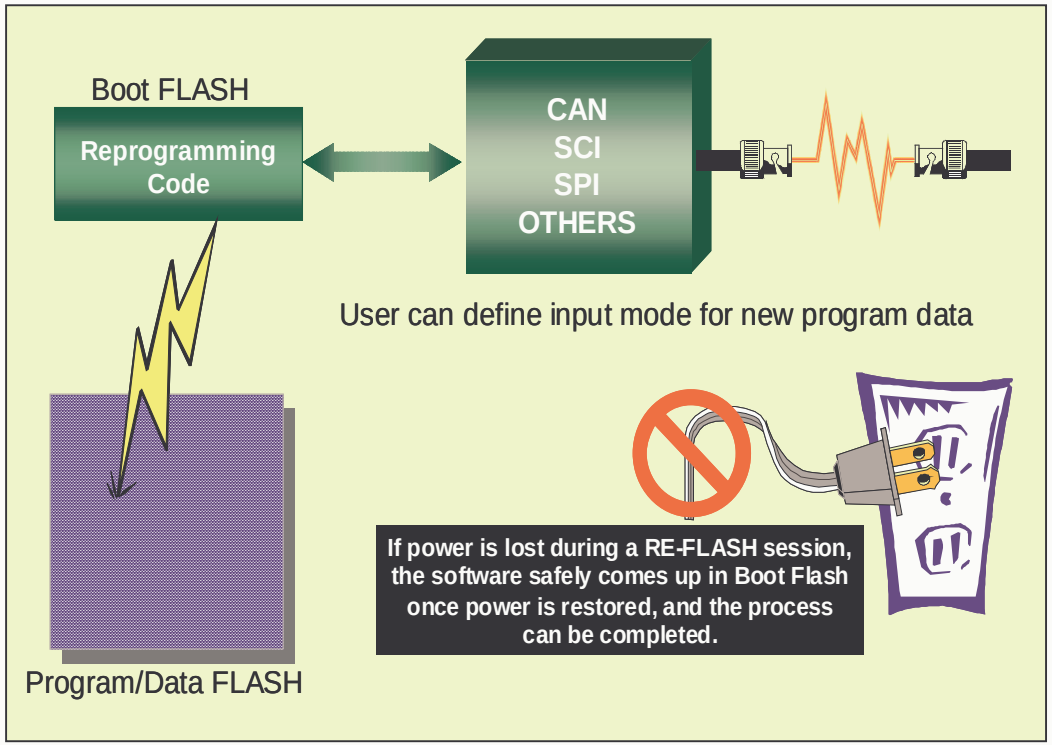


- ✓ On chip Harvard Architecture
  - ✓ Separate program and data buses
  - ✓ Permits up to three simultaneous accesses to program AND data memory
- ✓ On chip and Off-chip memory
  - ✓ Up to 128KBytes X data memory
  - ✓ Up to 128KBytes program memory
- ✓ 2Kx16 BootFLASH
  - ✓ 256 word page size
- ✓ Flash memory programmable via JTAG/OnCE interface or user program
- ✓ Programmable wait states for low cost system memory solutions

Available Memory

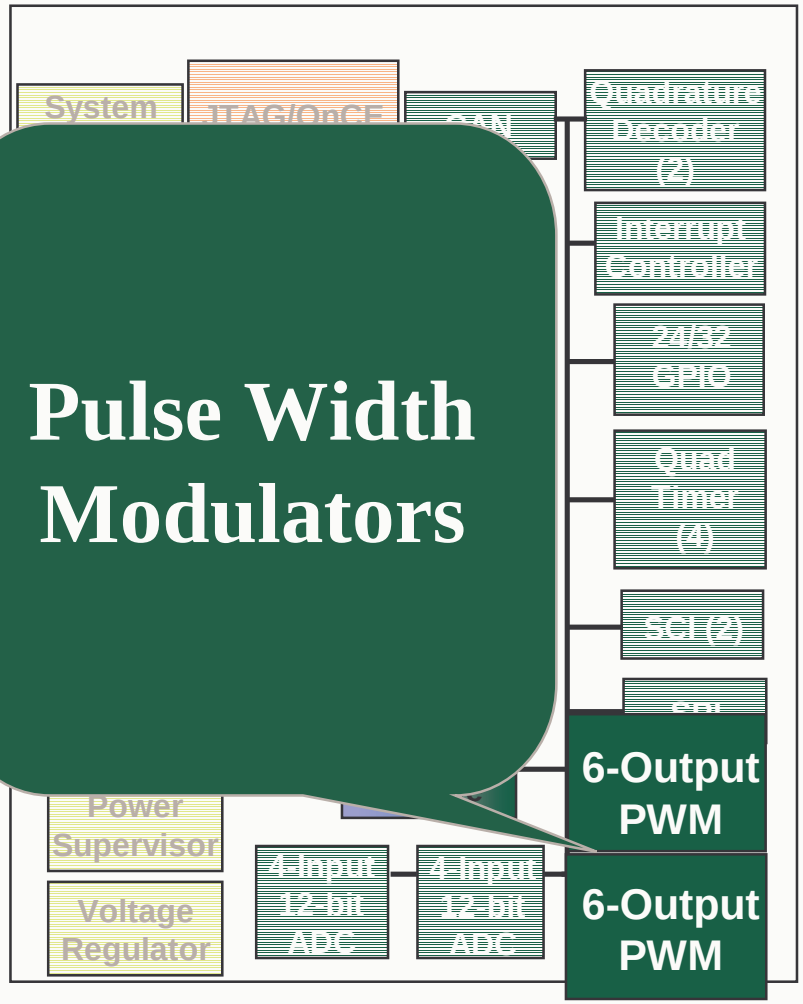
FEATURES	56F801	56F803	56F805	56F807	56824	56F826	56F827
Prog Flash (16-bit)	8K	31.5K		60K	-	31.5K	63K
Program ROM (16-bit)	-	-	-	-	32K	-	-
Prog RAM (16-bit)	1K	512		2K	128	512	1K
Data Flash (16-bit)	2K	4K		8K	-	2K	4K
Data ROM (16-bit)	-	-	-	-	2K	-	-
Data RAM (16-bit)	1K	2K		4K	3.5K	4K	4K
BootFLASH (16-bit)	2K				-	2K	-
Ext. Address Range	-	64K					
Ext. Data Bus Width	-	16-Bit					

User Defined FLASH Reprogramming



- Flash organized in rows of 32 words (512 bits)
- Endurance - 100 000 cycles
- Page Erase Capability - 512 bytes per page
- Page Erase Time – 40ms
- Access Time – 20ns
- Word Programme Time – 20us
- Serial Bootloader Available – downloads S-record files using terminal program

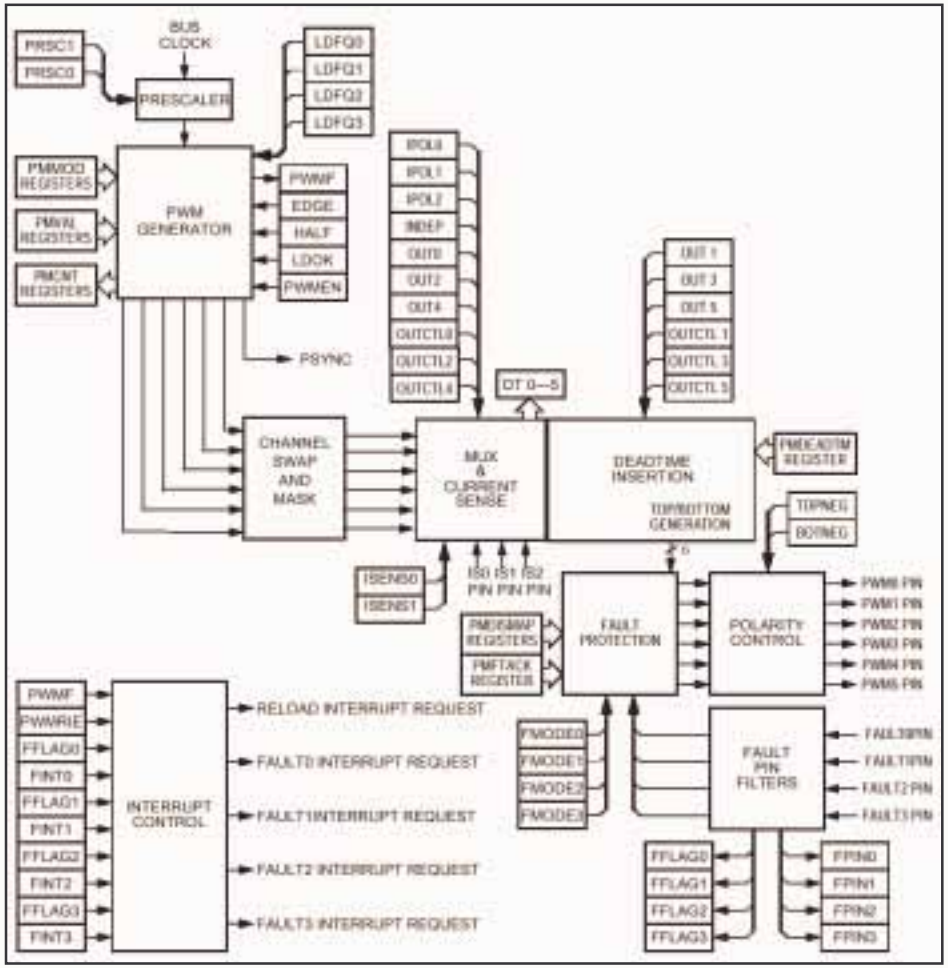
Pulse Width Modulators



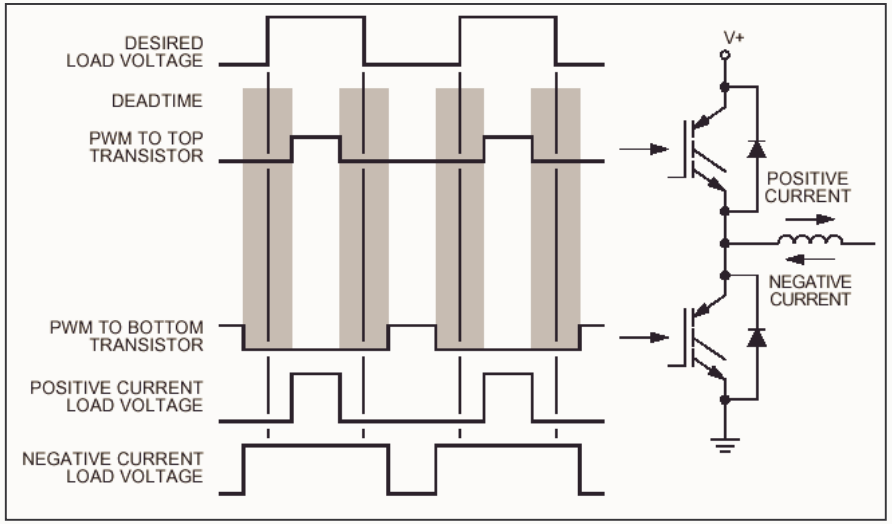
- ✓ Three complementary signal pairs or six independent signals
- ✓ Complementary channel operation
  - ✓ Deadtime insertion
  - ✓ Separate top and bottom pulse width correction via current sensing or software
  - ✓ Separate top and bottom polarity control
- ✓ Edge-aligned or center-aligned signals
- ✓ 15-bits of resolution
- ✓ Half-cycle reload capability
- ✓ Programmable integral reload rates (1 to 16)
- ✓ Individually programmable outputs
- ✓ Four programmable fault inputs
- ✓ 16 mA current sink capability
  10 mA current source
- ✓ Write protected registers
  - ✓ Protection for key parameters

Pulse Width Modulators

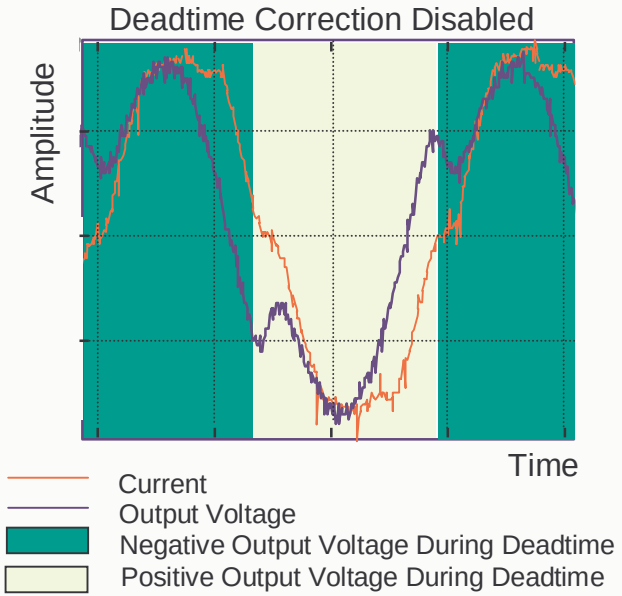
- Three complementary PWM signal pairs, or six independent PWM signals
- Features of complementary channel operation
  - — Deadtime insertion
  - — Separate top and bottom pulse width correction via current status inputs or software
  - — Separate top and bottom polarity control
- Edge-aligned or center-aligned PWM signals
- 15-bits of resolution
- Half-cycle reload capability
- Integral reload rates from one to 16
- Individual software-controlled PWM output
- Programmable fault protection
- Polarity control
- 20-mA current sink capability on PWM pins
- Write-protectable registers



PWM - Deadtime Distortion



- **Both transistors are off during deadtime**
- **Load inductance keeps current flowing through the diodes and thus creating an output voltage**
- **Positive current flow causes negative output voltage during deadtime – top transistor controls output voltage**
- **Negative current flow causes positive output voltage during deadtime – bottom transistor controls output voltage**



- **Causes poor low-speed motor performance**
- **Torque ripple**
- **Distorts current waveform**

PWM - Top/Bottom Correction

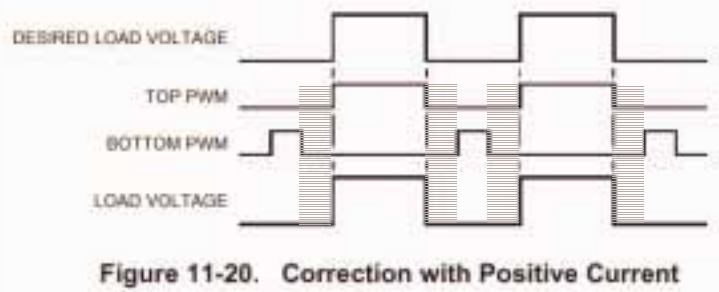


Figure 11-20. Correction with Positive Current

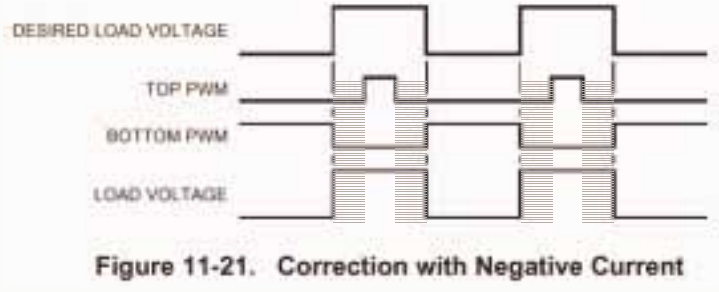
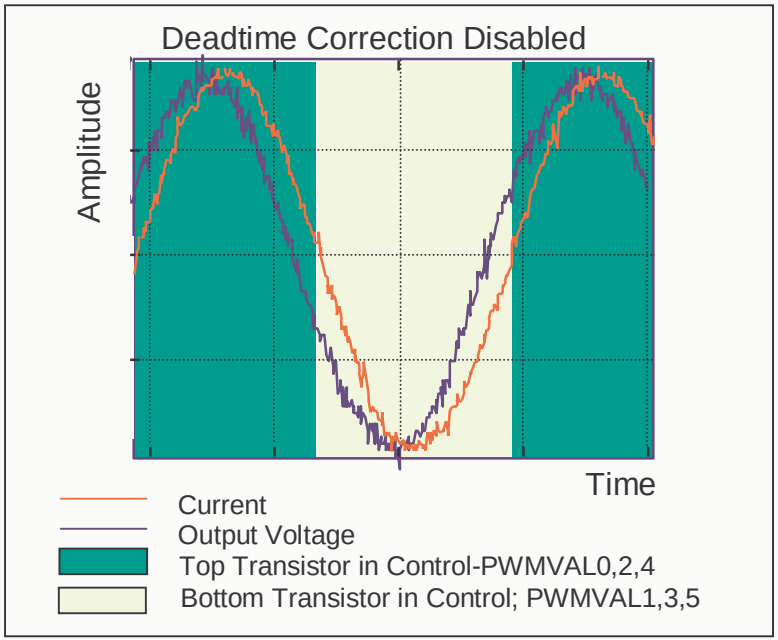


Figure 11-21. Correction with Negative Current

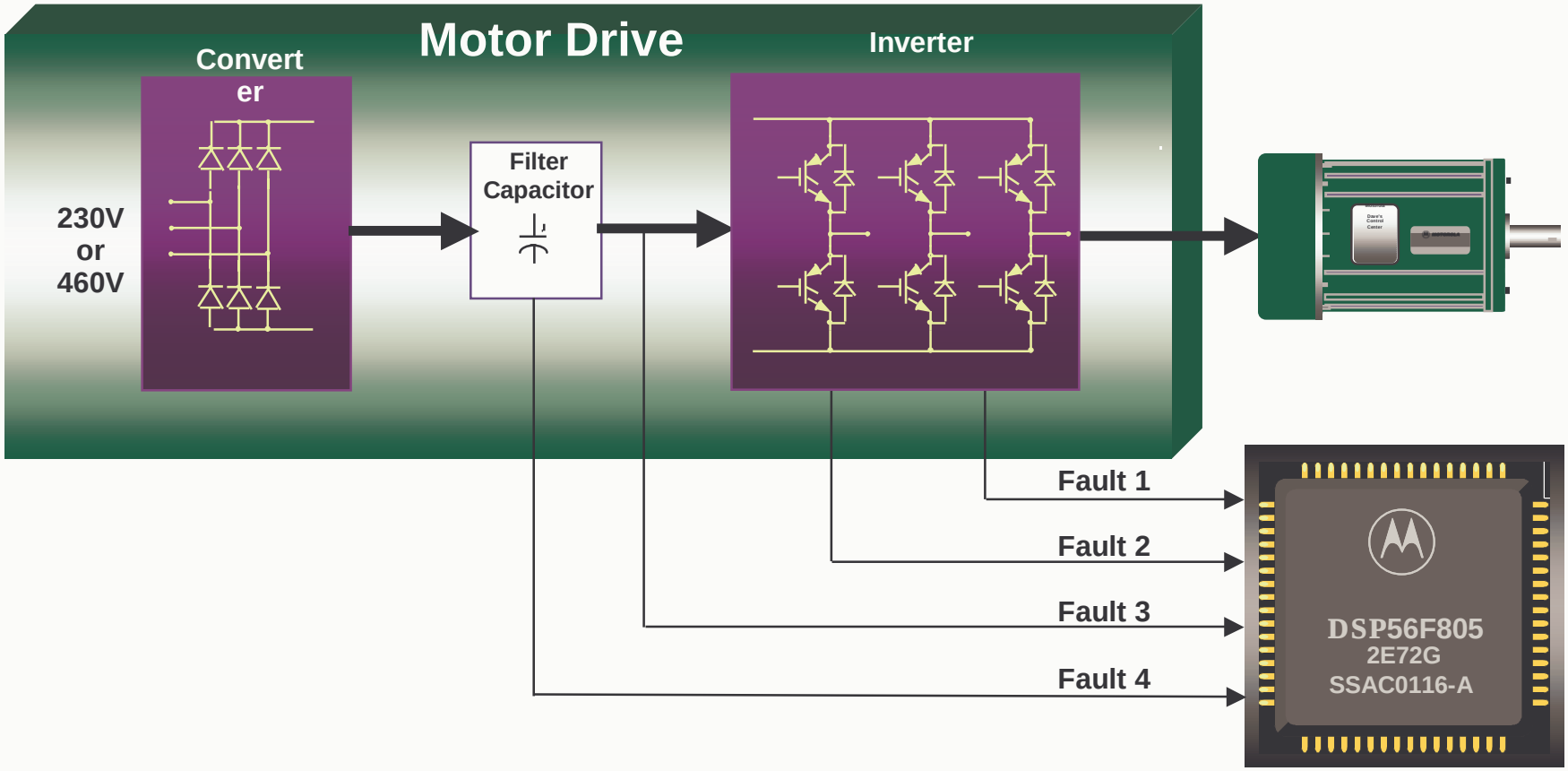


- **Reload PWMVAL0,2,4 by duty cycle + deadtime correction and use it if current is positive**
- **Reload PWMVAL1,3,5 by duty cycle - deadtime correction and use it if current is negative**
- **Type of corrections:**
  - **Manual**
  - **Automatic current status correction**

Top/Bottom Manual Correction

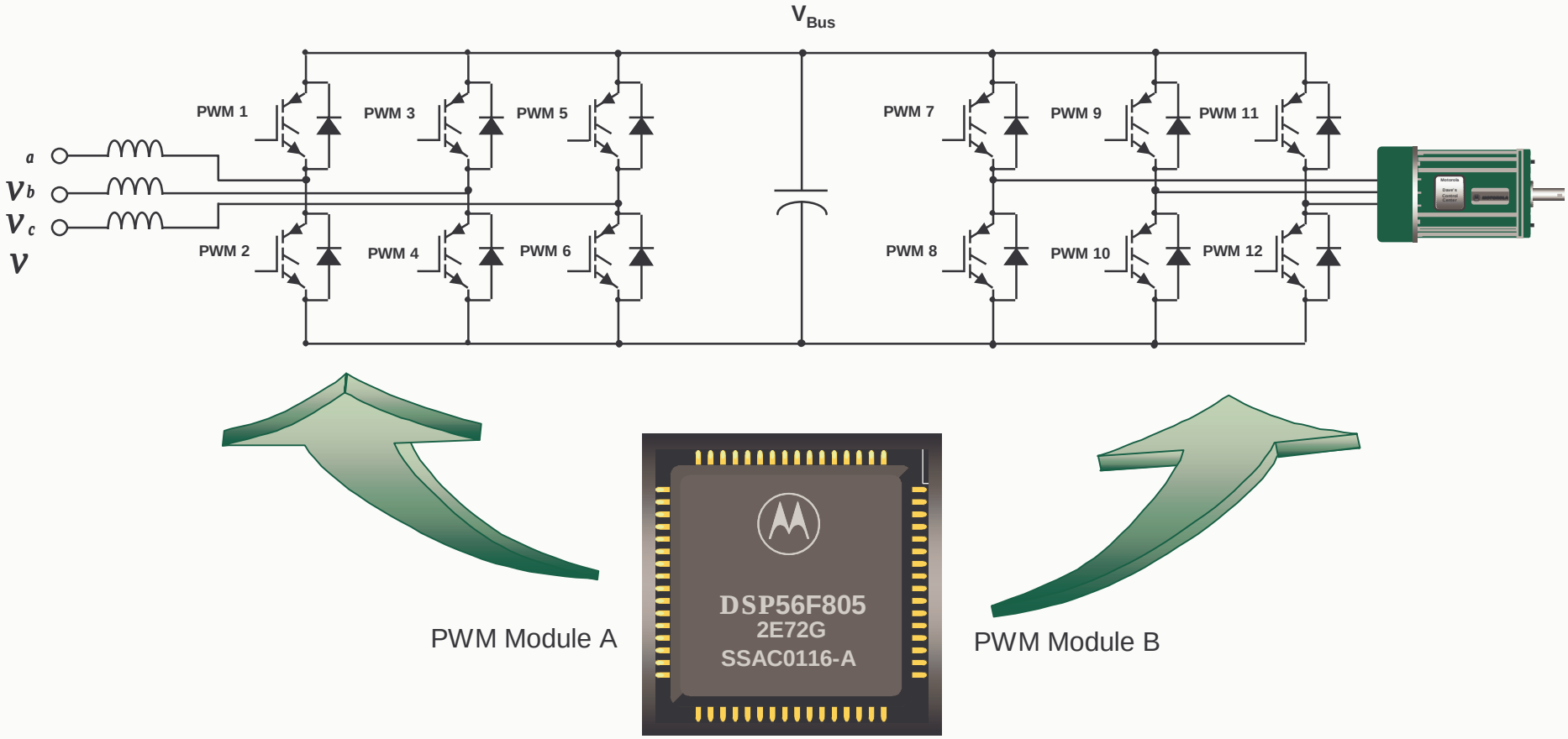
Bit	Logic state	Output control
IPOL0	0	PMVAL0 controls PWM01/PWM1 pair
	1	PMVAL1 controls PWM0/PWM1 pair
IPOL1	0	PMVAL2 controls PWM2/PWM3 pair
	1	PMVAL3 controls PWM2/PWM3 pair
IPOL2	0	PMVA45 controls PWM4/PWM5 pair
	1	PMVAL5 controls PWM4/PWM5 pair

Multiple Fault Inputs



- ✓ Fault inputs can independently monitor critical system parameters, and generate an interrupt when asserted.
- ✓ Each input is mappable to immediately disable any or all PWMs
- ✓ Each input is programmable to allow Automatic or Manual PWM restart.

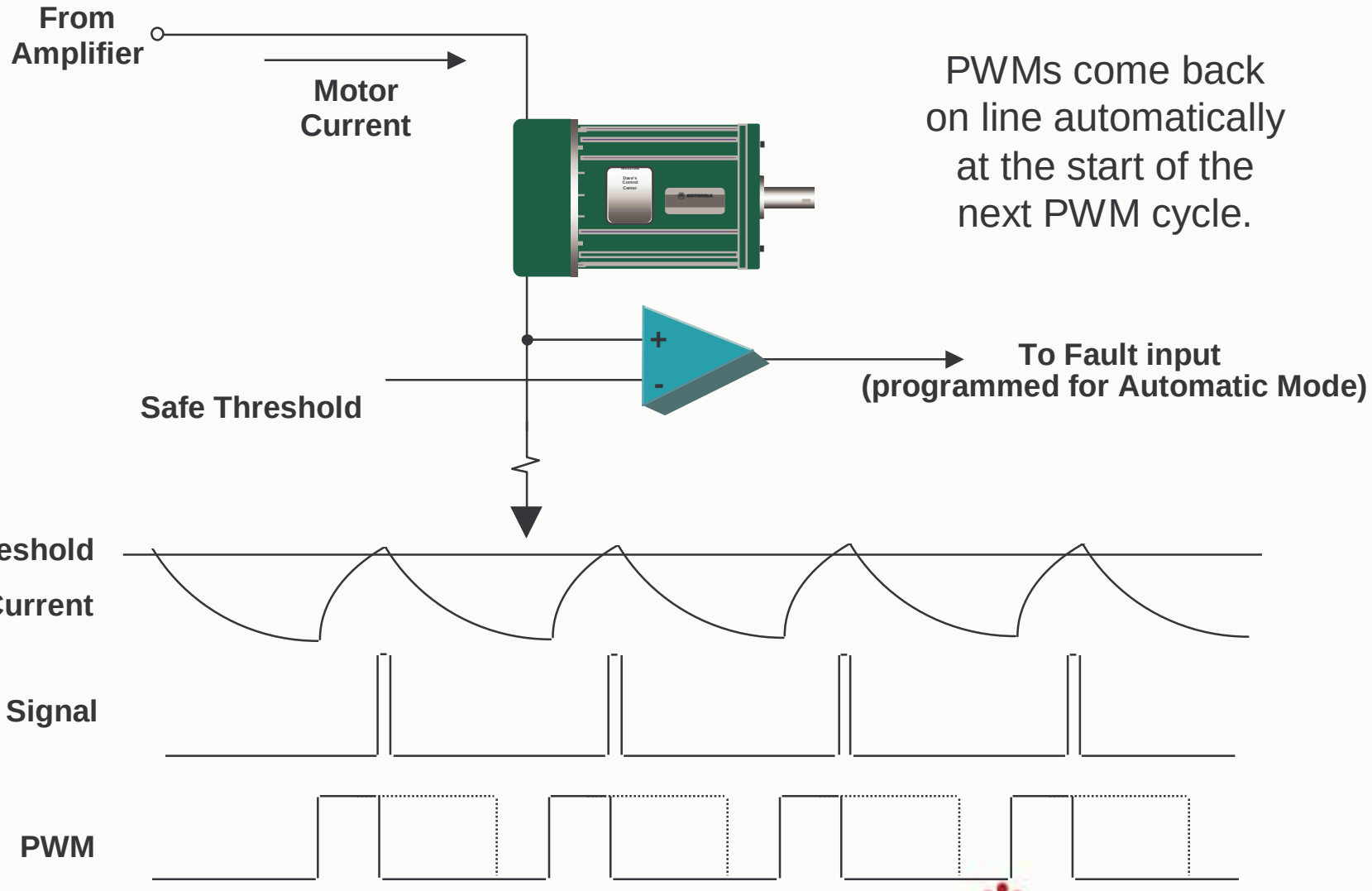
PWM - Separate Converter & Inverter Controls



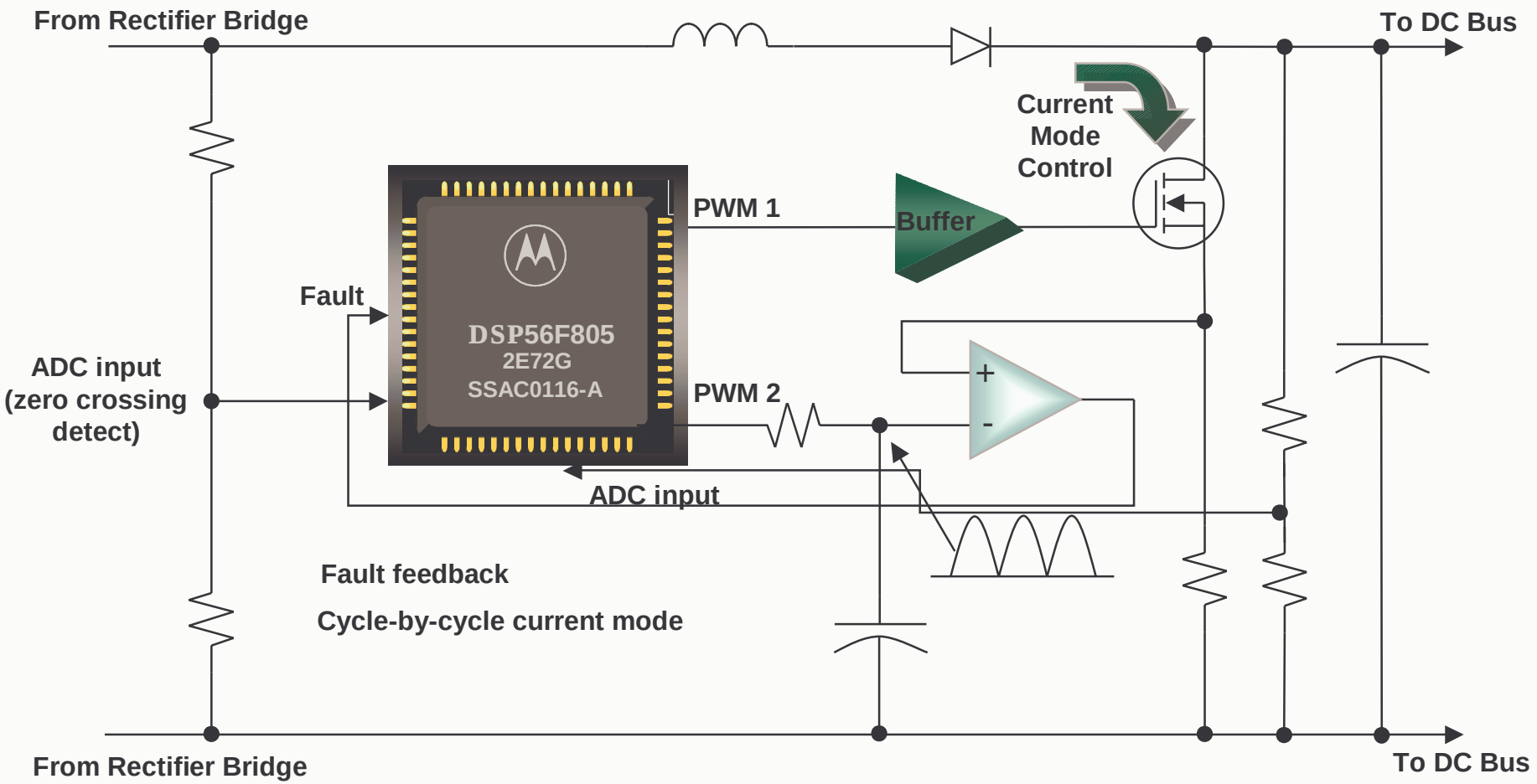
The advantages of intelligent control of the front end converter include:

- Tight bus voltage regulation, Bi-directional power flow based on regulation of the bus voltage
- Bus voltage boost from the input mains voltage, Unity power factor

Cycle-by-Cycle Current Limiting (Automatic PWM Restart)

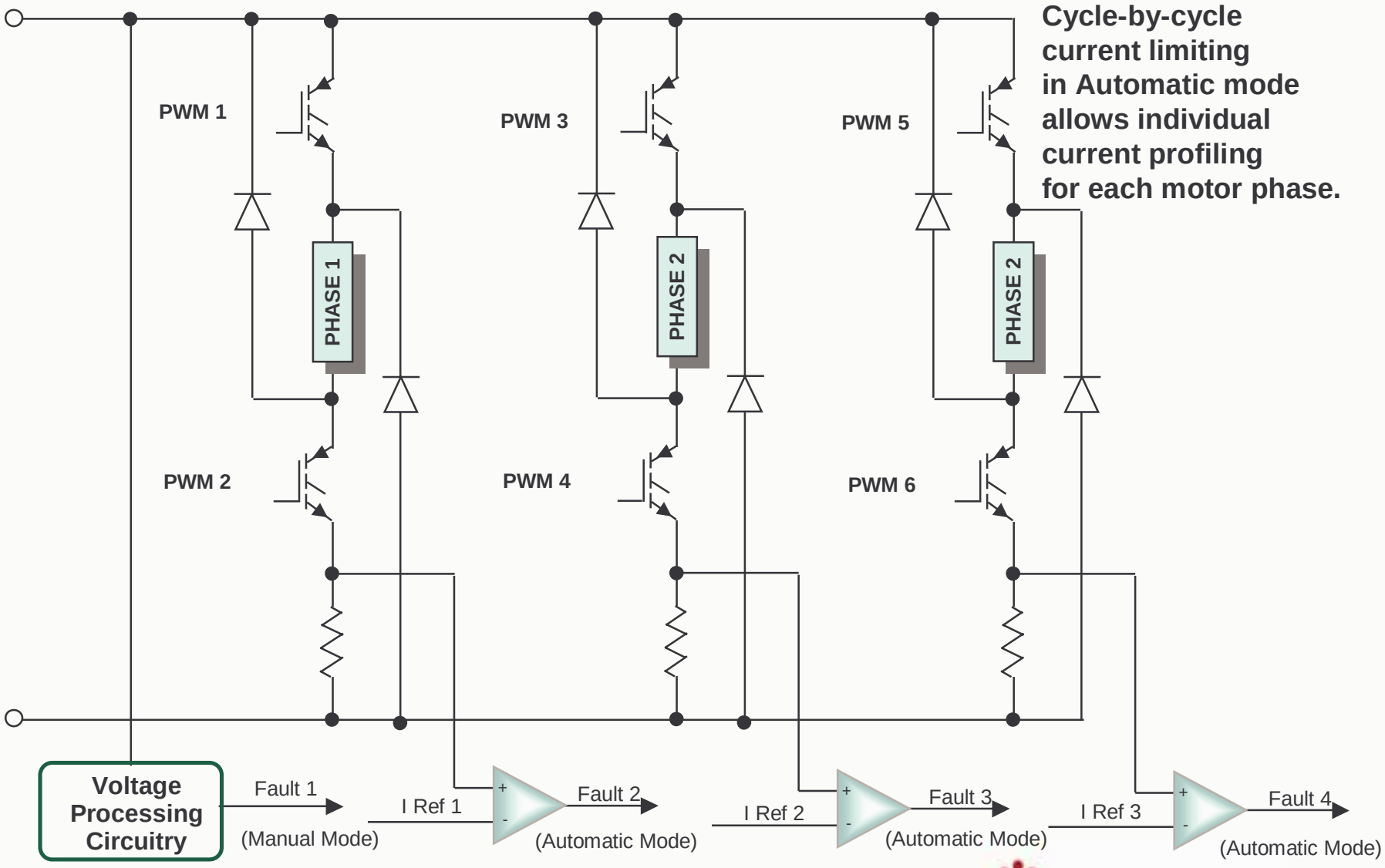


Single Phase PF Correction



Remaining PWM Module available for inverter control

SR Motor Control with Current Profiling

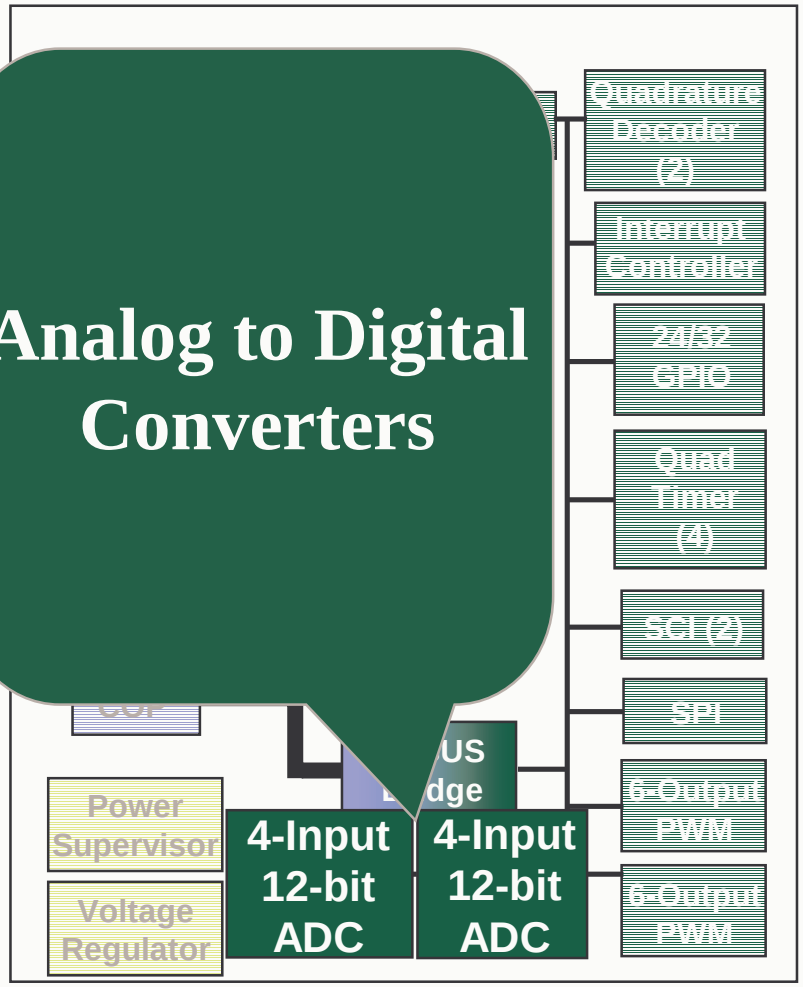


Cycle-by-cycle current limiting in Automatic mode allows individual current profiling for each motor phase.

“Write Once” System Protection

- ✓**Protects critical system configuration data from accidentally being changed**
- ✓**Parameters include:**
  - Dead-time value
  - Fault disable mapping
  - PWM output polarity bits
  - Independent or Complementary (tandem) PWM operation
- ✓**In a typical motor control application, these parameters are constants which are not expected to change for a given system configuration.**

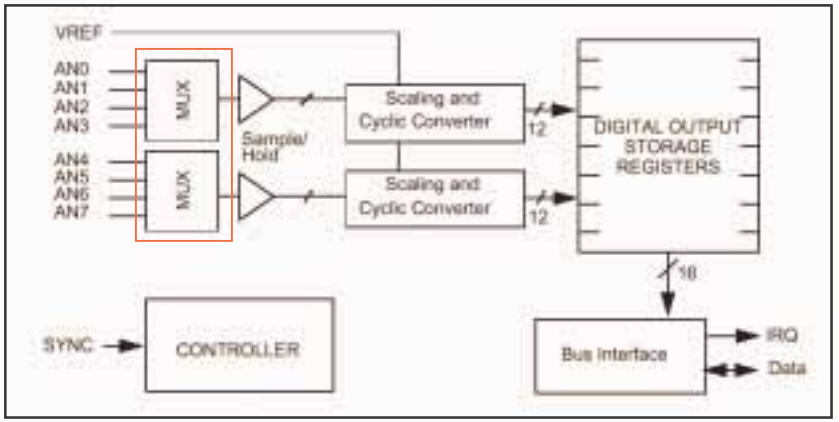
Analog to Digital Converters



- ✓ 12 bit resolution, 9 Bit accuracy
- ✓ Sampling rates up to 3.3 million / second
- ✓ Single conversion in 1.2 µsec
- ✓ 8 conversions in 5.3 µsec
- ✓ Can be synchronized with Pulse Width Modulators (PWM)
  - ✓ Provide simultaneous A/D conversion
- ✓ Sample correction via programmable offset
- ✓ Interrupt generating capabilities
  - ✓ End-of-Scan
  - ✓ Zero crossing
  - ✓ High/Low limit check
- ✓ Two outputs formats available
  - ✓ Two's complement
  - ✓ Unsigned

Analog to Digital Converter

- 12-bit resolution
- Sampling rate up to 1.66 million samples per second[1]
- Maximum ADC Clock frequency is 5MHz with 200 ns period
- Single conversion time of 8.5 ADC Clock cycles (8.5 x 200 ns = 1.7 µs)
- Additional conversion time of 6 ADC clock cycles (6 x 200 ns = 1.2 µs)
- Eight conversions in 26.5 ADC Clock cycles (26.5 x 200 ns = 5.3 µs) using Simultaneous mode
- ADC can be synchronized to the PWM via the SYNC signal
- Simultaneous or sequential sampling
- Internal multiplexer to select two of eight inputs
- Ability to sequentially scan and store up to eight measurements
- Ability to simultaneously sample and hold two inputs
- Optional interrupts at end of scan, if an out-of-range limit is exceeded or at zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned result
- Single ended or differential inputs



Allows simultaneous sampling of two selected channels

Two channels from the same group can be measured simultaneously if the channels are swapped

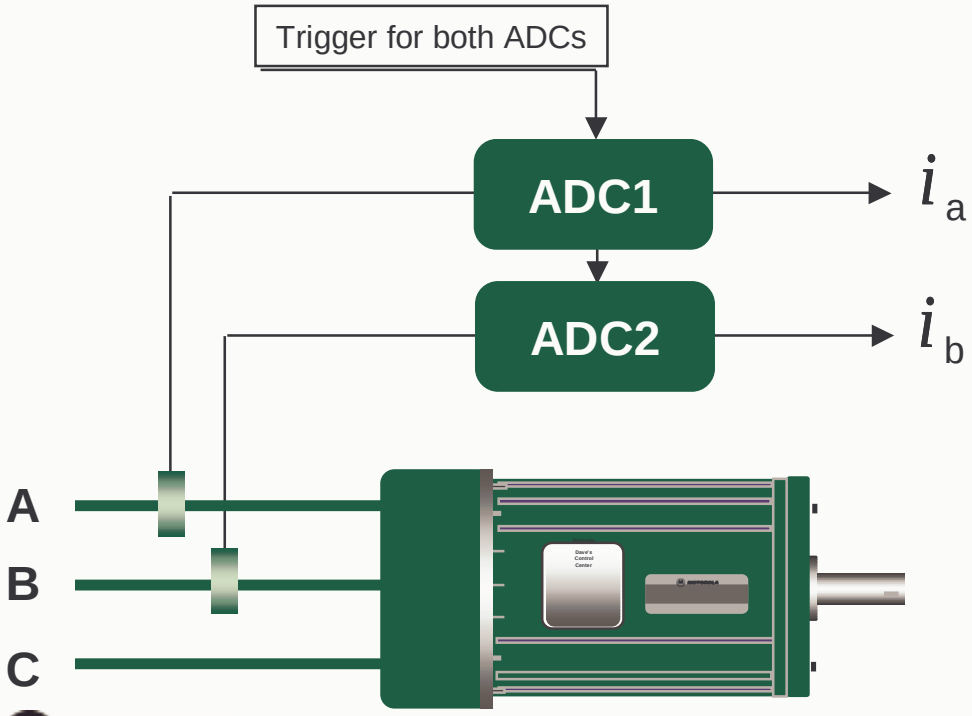
ADC – Interrupts & Scan Modes

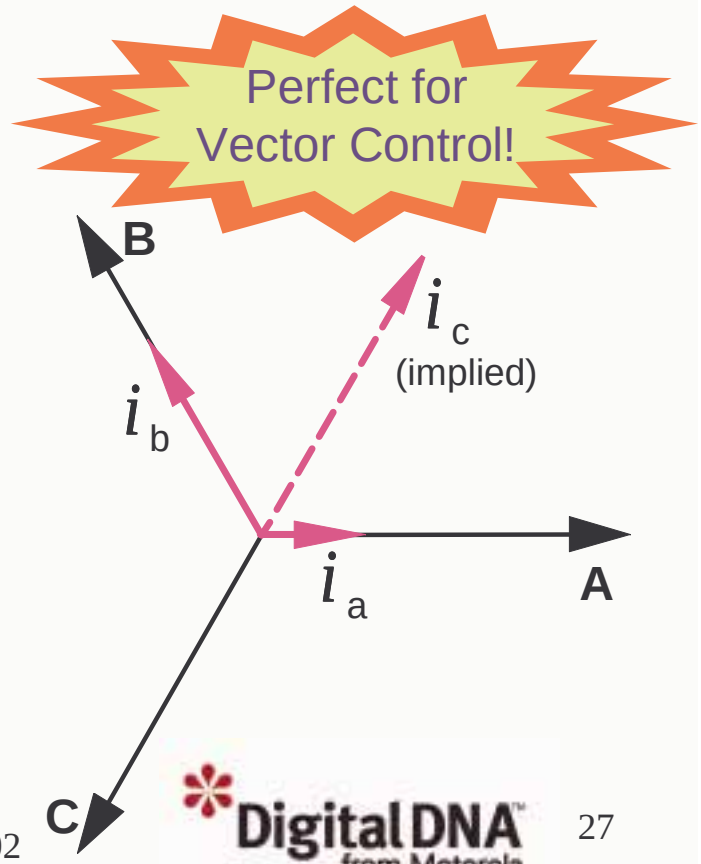
- **Generated Interrupts**
  - **End od Scan Interrupt Enable** – generated upon completion of any Scan and convert sequence, except for Loop Sequential or Loop Simultaneous modes
  - **Zero Crossing Interrupt Enable**
  - **High Limit Interrupt Enable**
  - **Low Limit Interrupt Enable**

- **Scan Modes**
  - **Once Sequential –** samples from SAMPLE0 to a first disabled channel
  - **Once Simultaneous –** samples two channels at time SAMPLE0/SAMPLE4 to a first disabled channels
  - **Loop Sequential –** samples selected channels in loop until STOP bit is set
  - **Loop Simultaneous –** samples selected two channels in loop until STOP bit is set
  - **Triggered Sequential –** sampling of single channels initiates with every recognized START command or SYNC pulse
  - **Triggered Simultaneous –** sampling of two channels initiates with every recognized START command or SYNC pulse

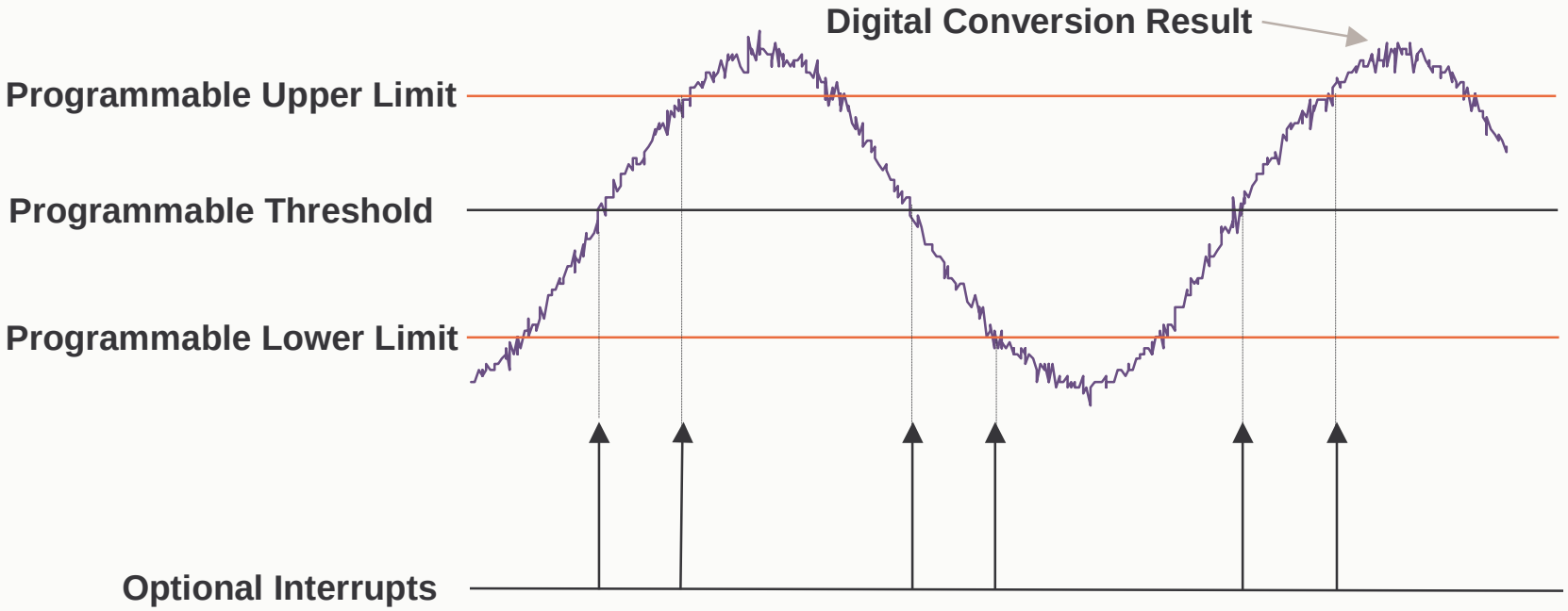
A to D Converters Designed for Motor Control

- ✓ 12 bit resolution at 2 uS conversion time
- ✓ Both ADCs can be triggered at the same time for simultaneous sampling
- ✓ Each ADC input is muxed to both ADCs, allowing simultaneous sampling with any other input.



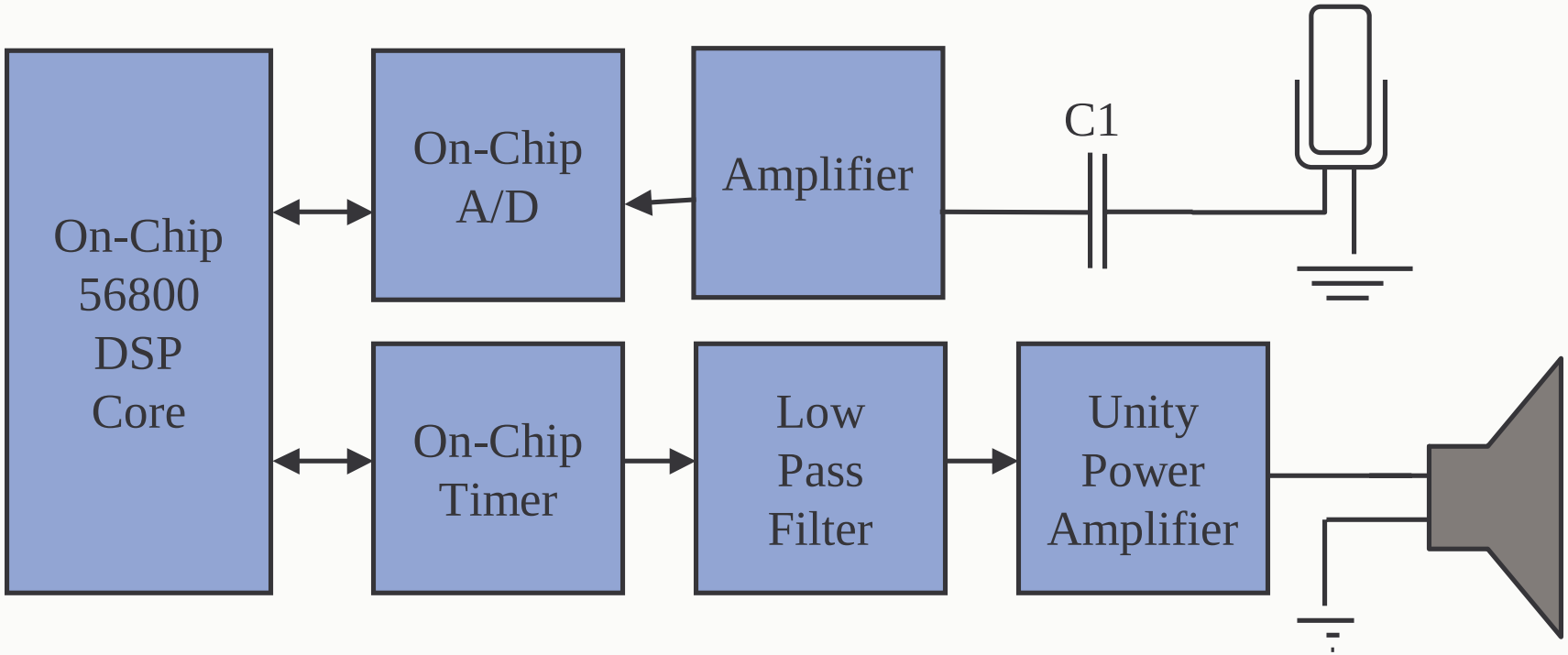


ADC Limit and Threshold Crossing Interrupts



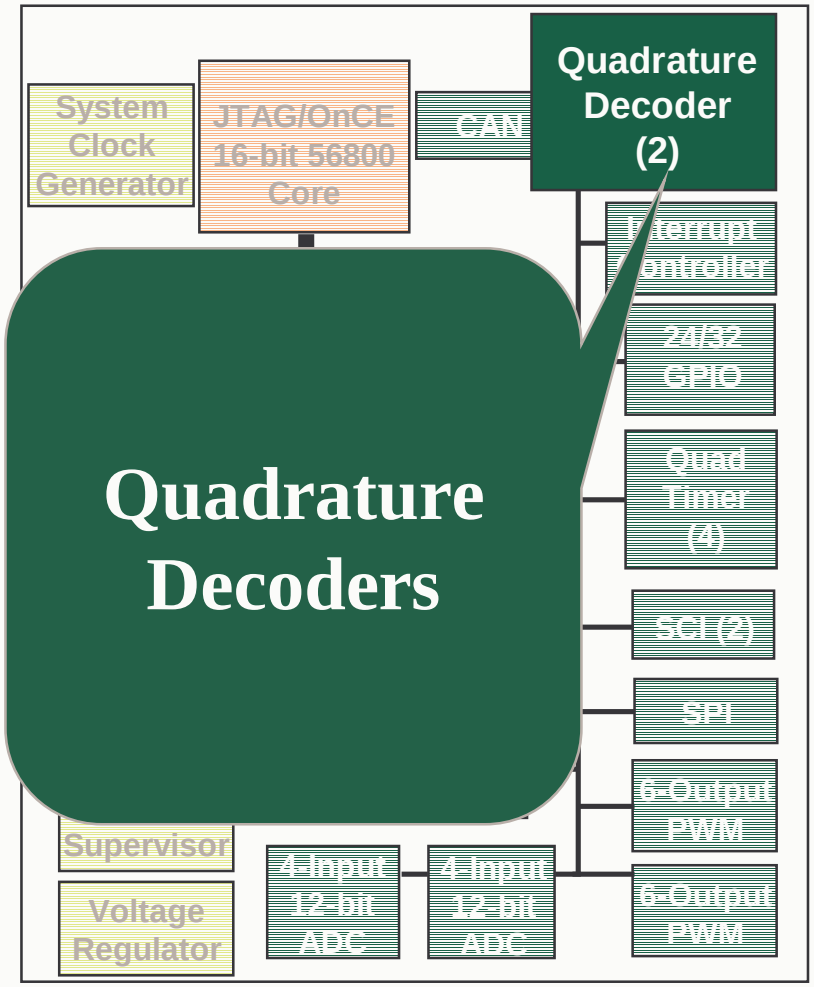
- ✓ The ADC can perform limit checking and zero crossing detection with NO CPU intervention.
- ✓ Each channel has its own upper, lower, and threshold comparators

A/D and PWM provide Low Cost CODEC functionality:



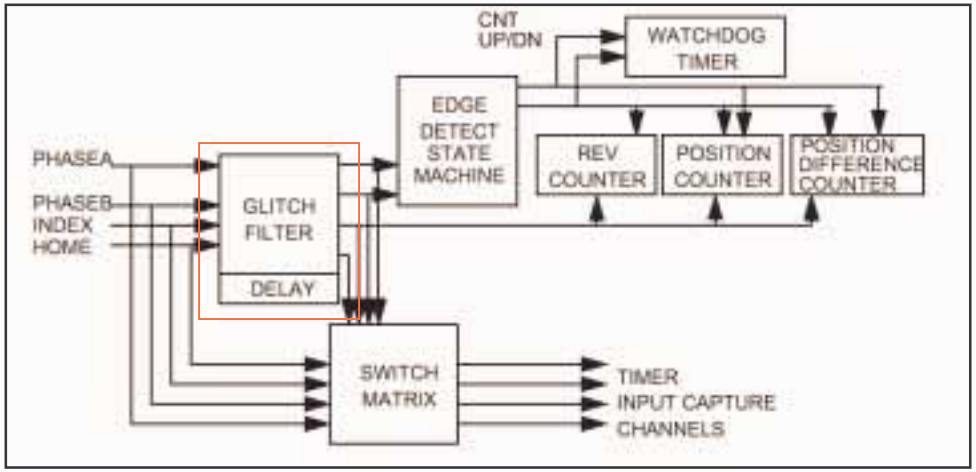
** See Appendix C for details.*

Quadrature Decoders



- ✓ Two encoder inputs per decoder
- ✓ Captures all four transitions on two-phased inputs
  - ✓extracts actual shaft position and direction
  - ✓32-bit position counter - initialized by software or external events
  - ✓Preloadable 16-bit revolution register
- ✓ Index input
  - ✓resets the current integration value
  - ✓begins integrating a new revolution value
- ✓ Configurable glitch filter for inputs
- ✓ Can operate as single-phase pulse accumulators
- ✓ Watchdog timer detects non-rotating shaft condition

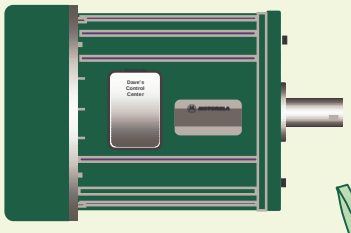
Quadrature Decoders



- **Samples four time points on the signal and verifies the majority of the signal level before outputting the new state to the internal logic**
- **Sample rate is fully programmable**

- Includes logic to decode quadrature signals
- Configurable digital filter for inputs
- 32-bit position counter
- 16-bit position difference register
- Maximum count frequency equals the peripheral clock rate
- Position counter can be initialized by SW or external events
- Preloadable 16-bit revolution counter
- Inputs can be connected to a general purpose timer to aid low speed velocity measurements
- Quadrature decoder filter can be bypassed
- A watchdog timer to detect a non-rotating shaft condition

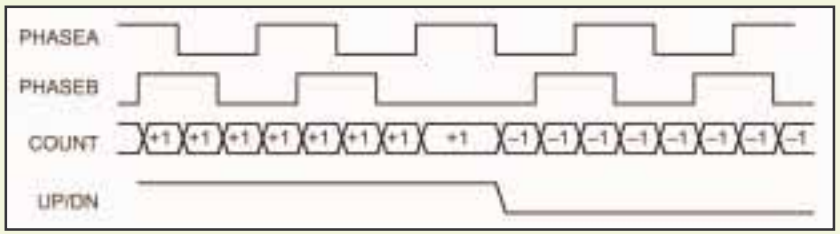
QD - Encoder Interface Features



Channel A
Channel B
Index

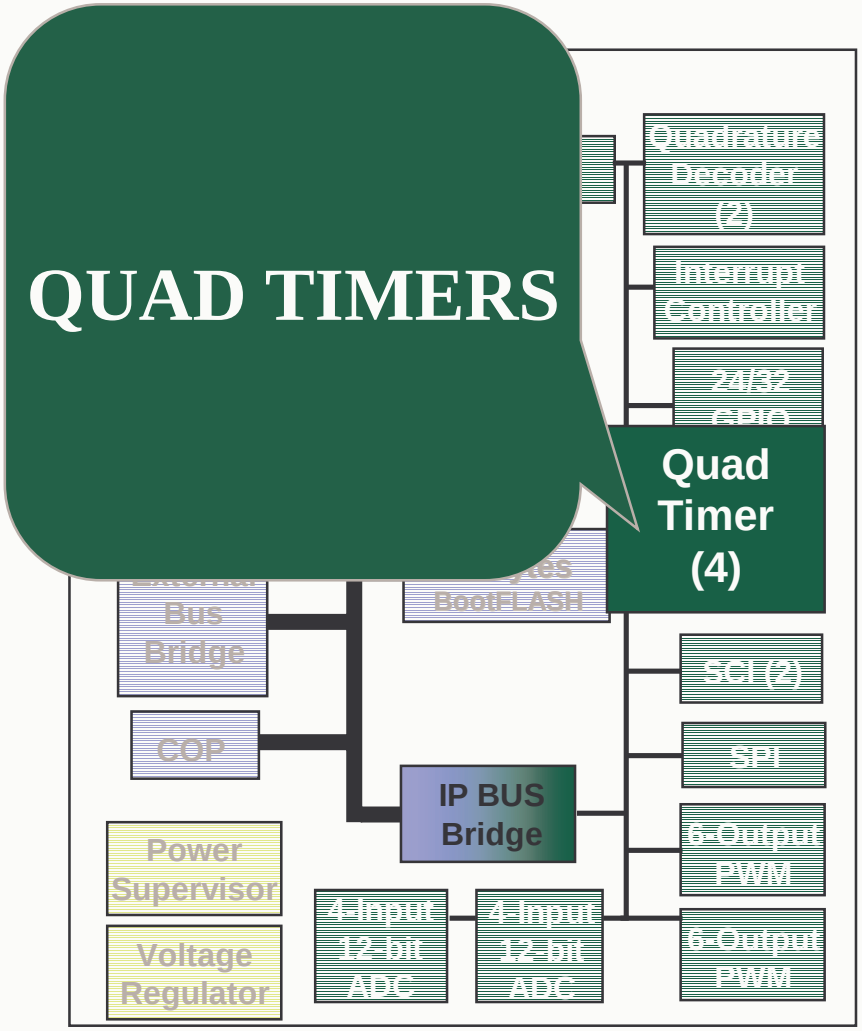
Home limit switch

Encoder Module



- Digital filtering on all inputs with programmable response time
- 32 bit bi-directional position tracking
- 16 bit revolution counter based on index signal
- 16 bit “delta count” velocity measurement
- “1/x” velocity measurement based on signal period
- “No rotation” watchdog interrupt w/ programmable timeout
- Optional interrupt on home or index signal
- Optional initialization of position on home or index signal

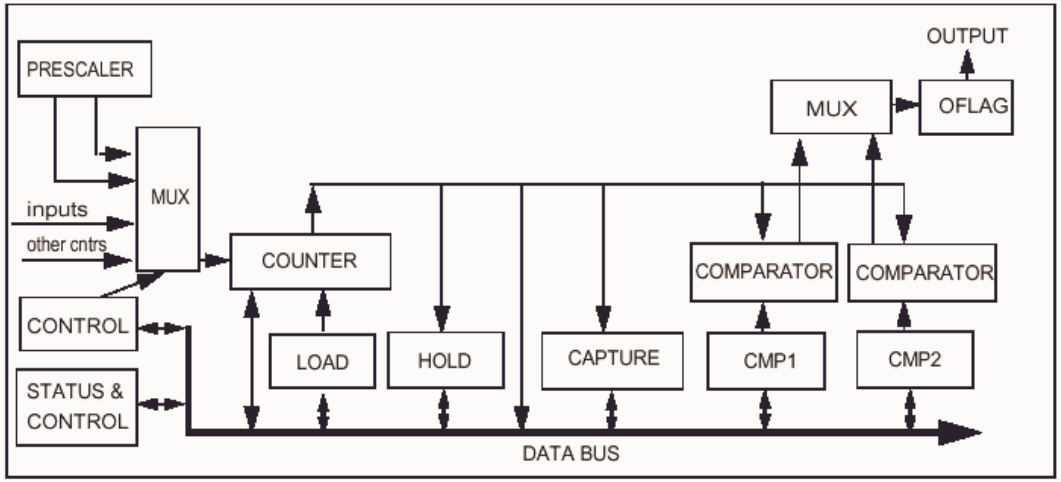
Quad Timers



- ✓ Sixteen -- 16-bit general purpose up/down timers
- ✓ Individually programmable
  - ✓ Input capture trigger
  - ✓ Output compare capture
  - ✓ Clock source
- ✓ Pins available as general I/O when timer(s) not in use
- ✓ Input pins are shareable within a timer module (Quad)
- ✓ Counters in a timer module can be daisy-chained to yield longer counter lengths

Quad Timers

- Each timer module consists of four 16-bit counters/timers
- Count up/down
- Counters are cascadable
- Programmable count modulo
- Max count rate equals peripheral clock/2 when counting external events
- Max count rate equals peripheral clock when using internal clocks
- Count once or repeatedly
- Counters are preloadable
- Counters can share available input pins
- Each counter has a separate prescaler
- Each counter has capture and compare capability

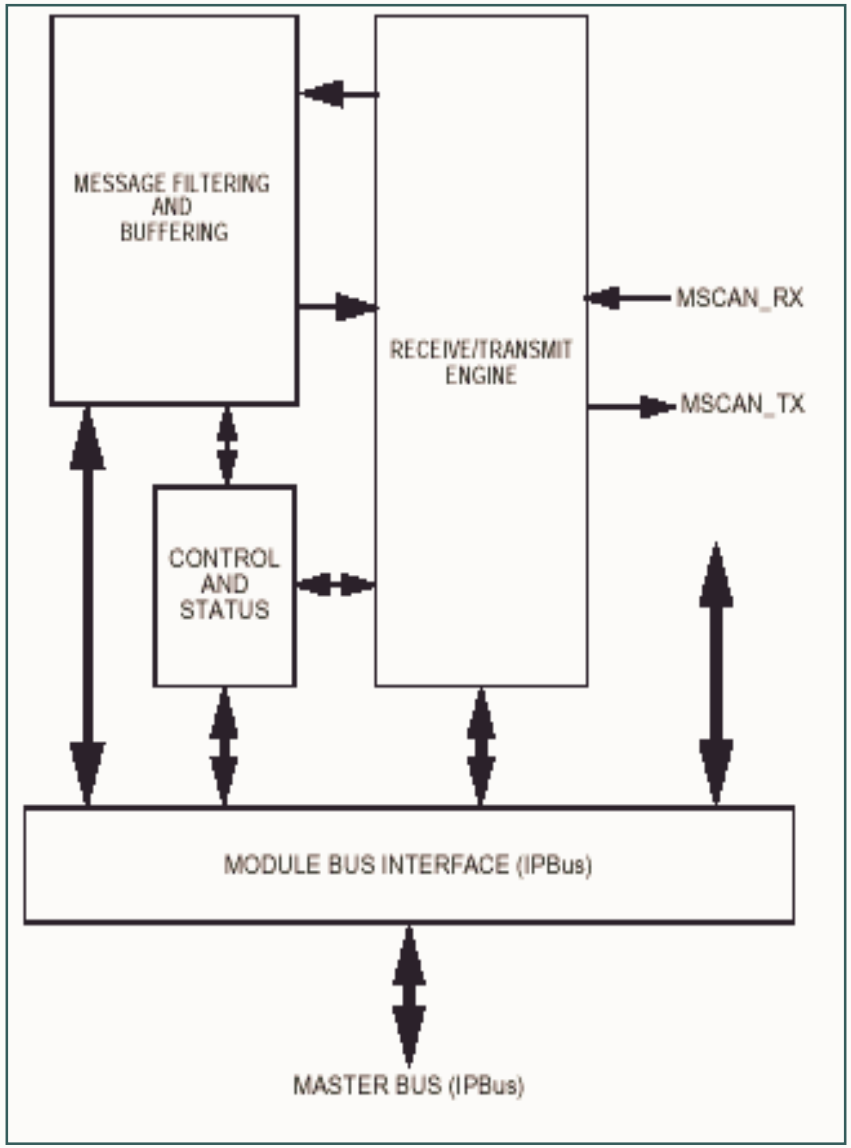


QT – Modes of Operation

Counting Mode Definitions

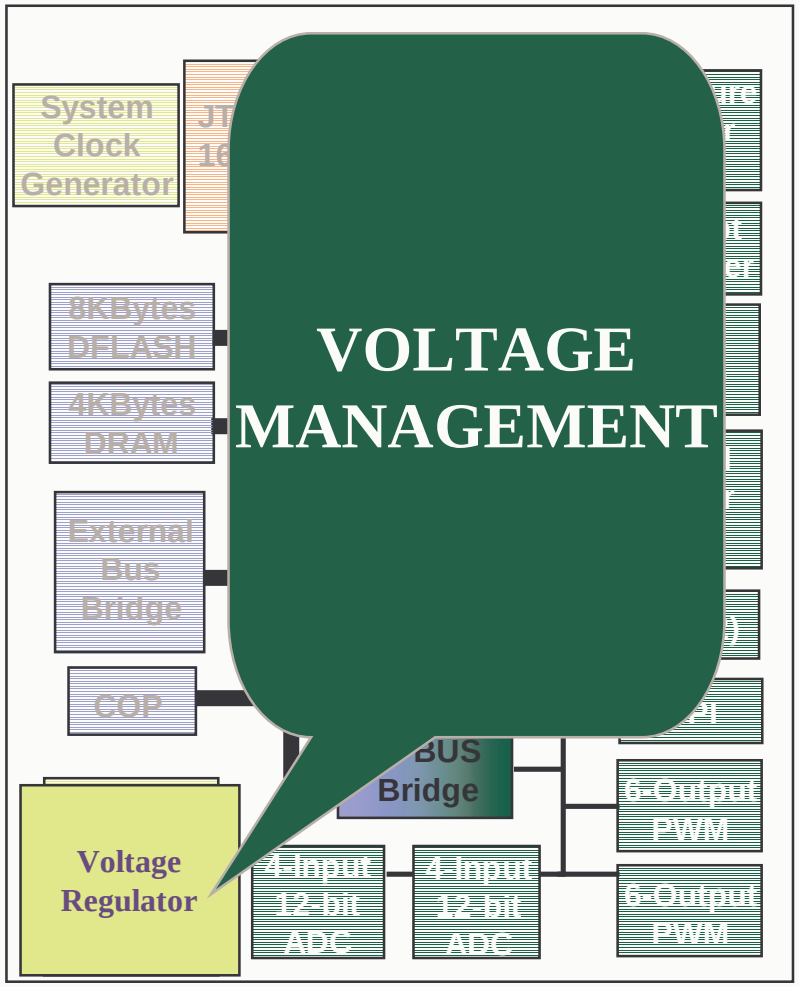
1. **Count Mode** – counts on rising edges (generating periodic interrupts, timing purposes)
2. **Edge-Count Mode** – count edges (counting of simple encoder wheel)
3. **Gated-Count Mode** – counts primary input signal if signal on secondary input is high (signal width measurement)
4. **Quadrature-Count Mode** – counter will decode the primary and secondary external inputs as quadrature encoded signals (movement monitoring)
5. **Signed-Count Mode** – counter increments/decrements accordingly to level of signal asserted on secondary source
6. **Triggered-Count Mode** – counts primary clock source if rising edge of the secondary input detected and stops counting if either rising edge or compare event occurs
7. **One-Shot Mode** – provides timing delays (ADC acquisition of new samples until a specified period of time has passed since the PWM sync signal)
8. **Cascade-Count Mode** – if any counter is read the values of other counters are captured in hold registers
9. **Pulse-Output Mode** – supports step motor systems and provides change of signal frequency and number of pulses
10. **Fixed- Frequency PWM Mode** – fixed frequency variable duty cycle generation (driving PWM amplifiers)
11. **Variable-Frequency PWM Mode** – variable frequency and duty cycle generation (driving PWM amplifiers)

56F807/05/03 Controller Area Network Module



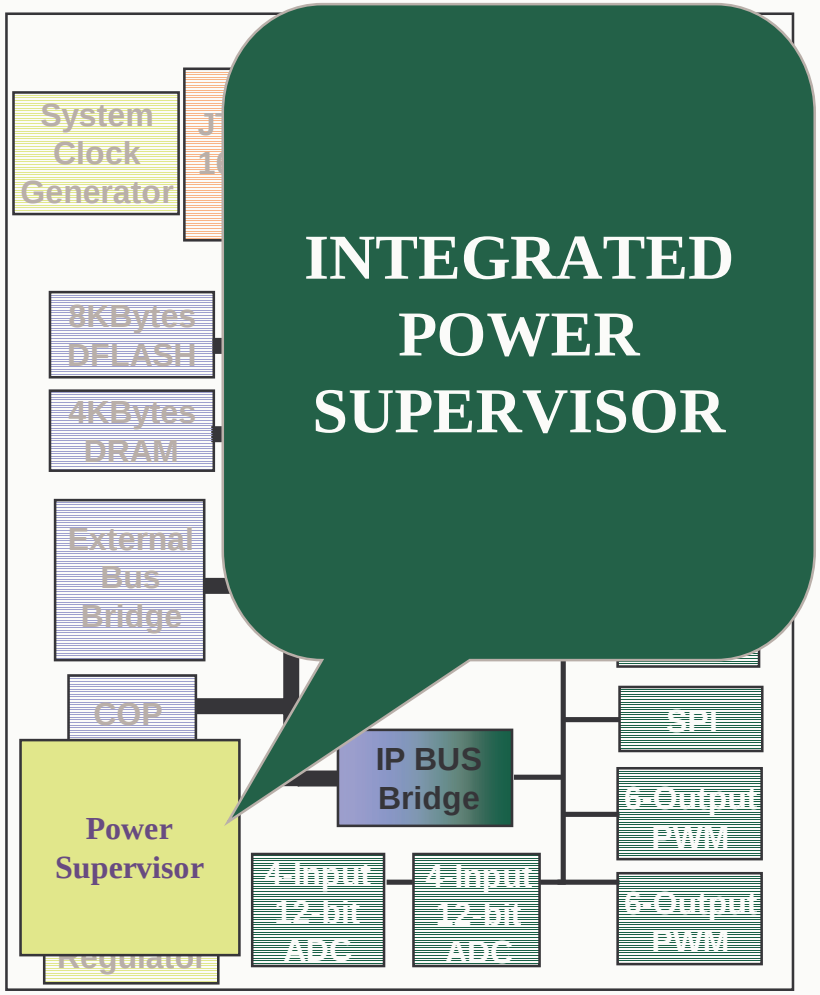
- Modular architecture
- Implementation of the CAN protocol—Version 2.0A/B
  - — Standard and extended data frames
  - — Zero to eight bytes data length
  - — Programmable bit rate up to 1Mbps
  - — Support for remote frames
- Double-buffered receive storage scheme
- Triple-buffered transmit storage scheme with internal prioritization using a *local priority* concept
- Flexible identifier filter capable of masking supports two full-size extended identifier filters: two 32-bit, four 16-bit, or eight 8-bit filters
- Programmable wake-up functionality with integrated low-pass filter
- Programmable Loop Back mode supports self-test operation
- Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states: Warning, Error Passive, Bus-Off
- Programmable MSCAN clock source, either IPBus clock or crystal oscillator output
- Three low power modes: Sleep, Soft Reset and Power Down

Voltage Management



- ✓ I/O drivers designed to interface at 3.3v (5v tolerant)
- ✓ Two internal regulators available
  - ✓ One for logic
  - ✓ One for analog
- ✓ Regulators converts 3.3V input to 2.5V internal operating voltage
  - ✓ Reduces overall system cost
  - ✓ Controls power usage
  - ✓ Controls system noise floor

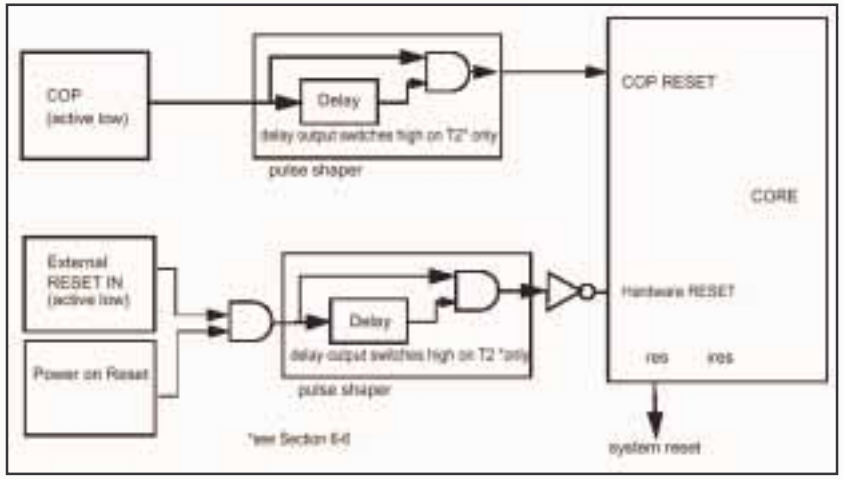
Integrated Power Supervisor



- ✓ Holds device in reset until there is enough voltage for on-chip logic to operate at the oscillator frequency
  - ✓ Precludes any problems associated with false restart
- ✓ Low Voltage Detect high-priority interrupt
  - ✓ Two low voltage detect signals used to initiate a software controlled shutdown when the supply voltage drops below acceptable levels
- ✓ Reduced system cost
  - ✓ Eliminates need for external power monitor

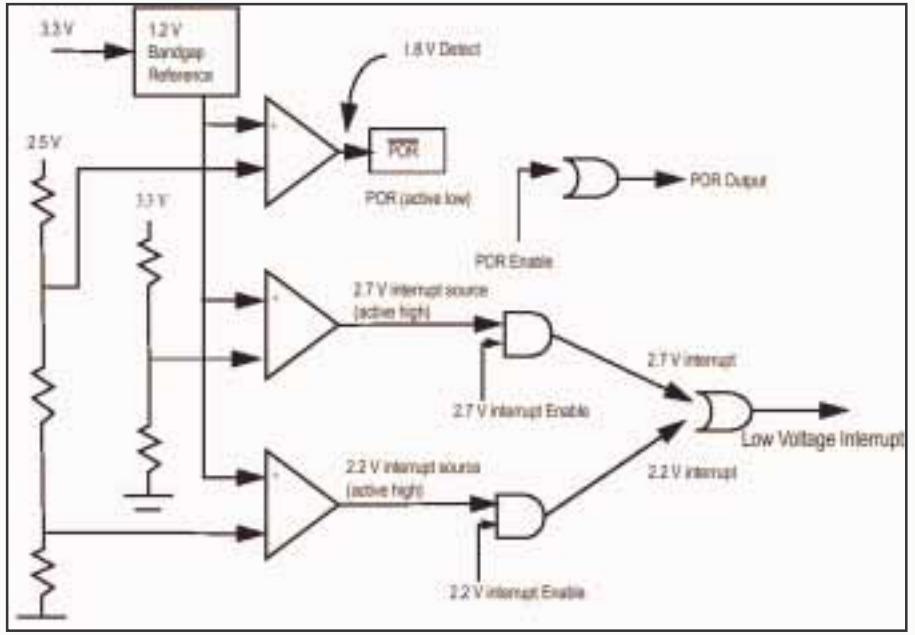
Reset, Low Voltage, COP

•Sources for Reset



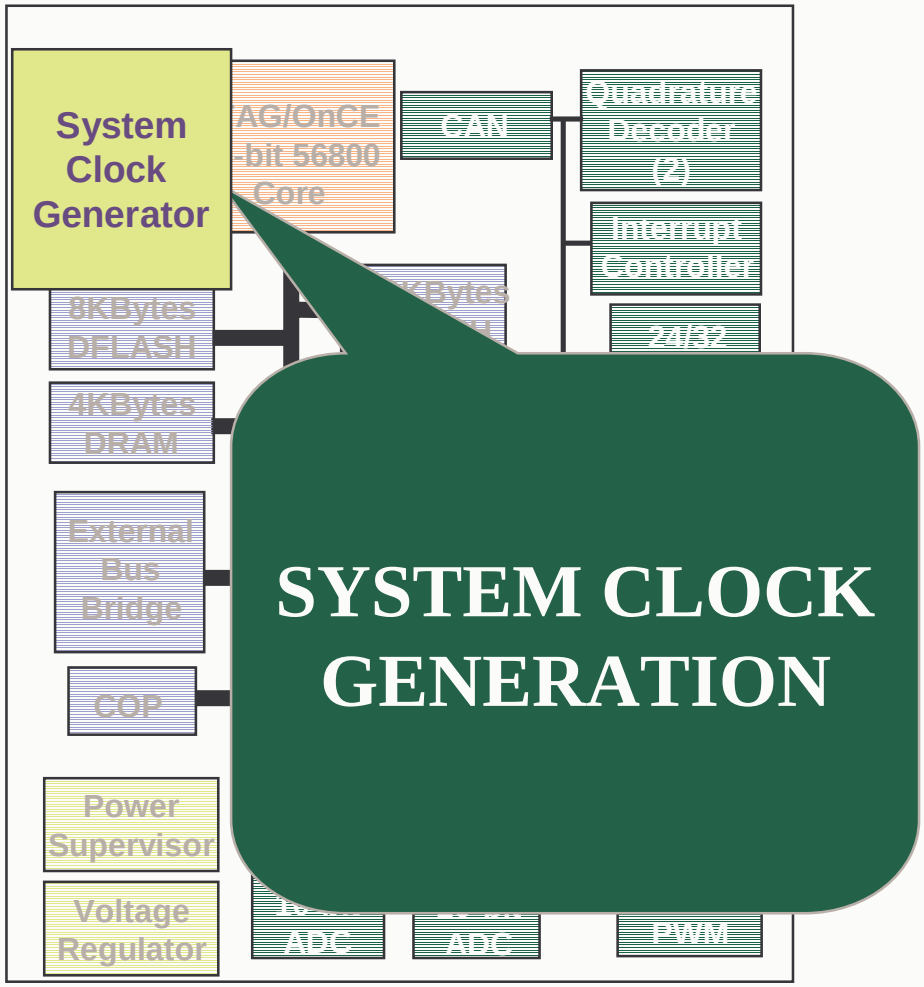
- **Computer Operating Properly (COP)** – software must periodically service the COP in order to clear the counter and prevent reset
- **COP Periods** - minimum 205us and maximum 839 ms at 80 MHz
- **Pulse Sharper** – force internal reset signal to be minimum of the 32 oscillator cycles

•Low Voltage Detection



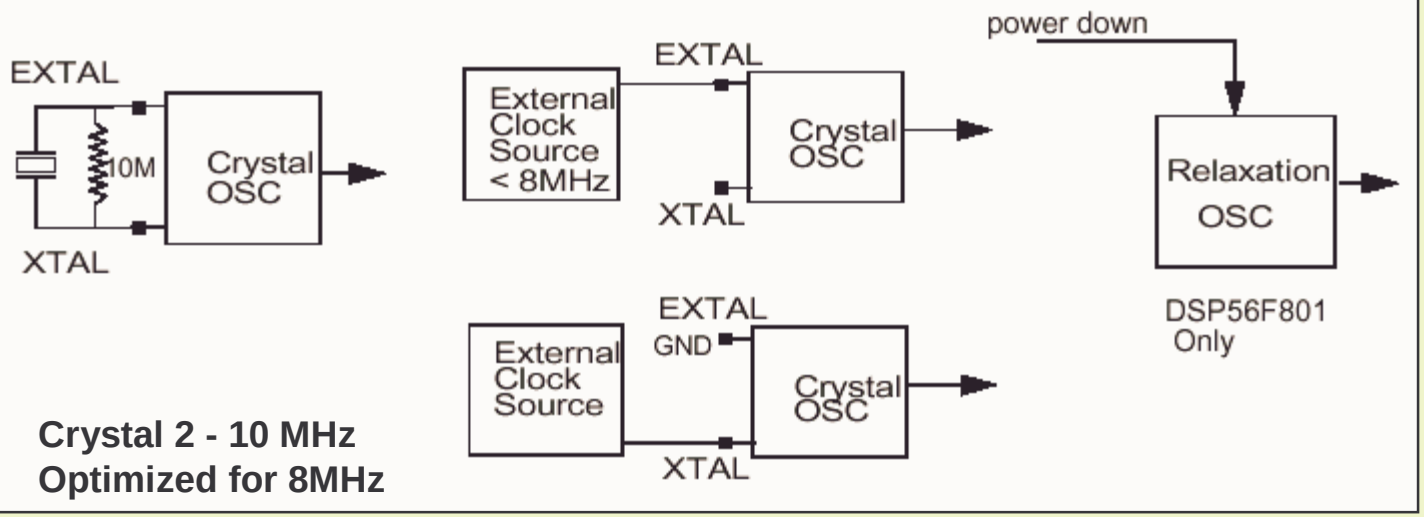
- **Power On Reset (POR)** – asserts internal reset from VDD=0V to VDD=1.8V
- **High Speed Operation** – requires inactive Low Voltage Interrupt otherwise DSP Core is able to run at the oscillator frequency

System Clock Generation



- ✓ Three different, dynamically selectable system clock sources available
  - ✓ Crystal Oscillator - driven by external crystal or clock source
  - ✓ Programmable 4-bit Prescaler - divide-by of the IP Bus clock
  - ✓ Phase Locked Loop (PLL) - generates output frequencies of up to 80 MHz
- ✓ Selectable Phase Locked Loop input clock source
  - ✓ Crystal Oscillator
  - ✓ Programmable 4-bit Prescaler
- ✓ Dynamically programmable PLL allows configurable power/speed options

System Clock Generation

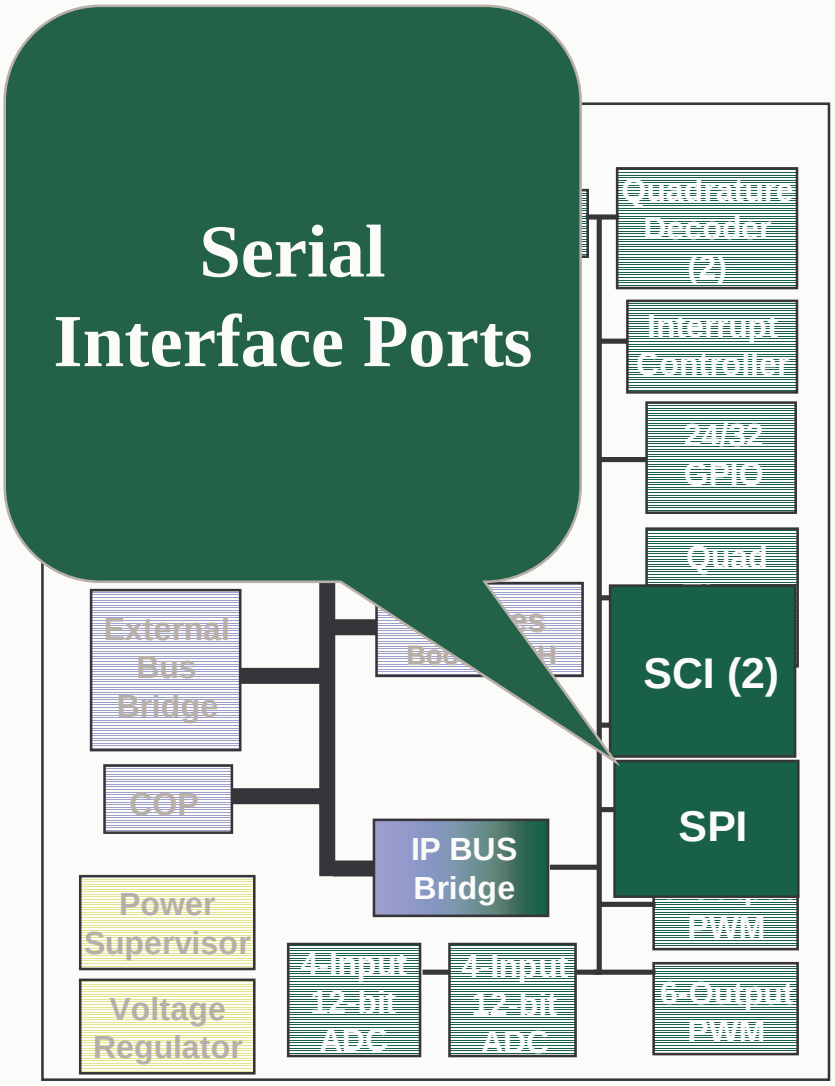


The On-chip Clock Synthesis (OCCS) module interfaces to the Oscillator and PLL and has an on-chip Prescaler. The OCCS Module features are as follows:

- 2-bit Prescaler
- 2-bit Postscaler
- Ability to power down the internal PLL
- Selectable PLL source clock
- Selectable system clock (ZCLK) from three sources

The clock generation module provides the programming interface for both the PLL and on and off-chip oscillators.

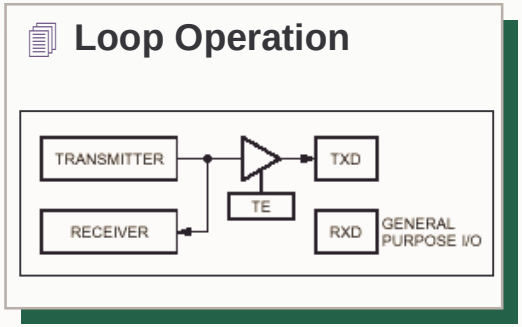
Serial Interface Ports

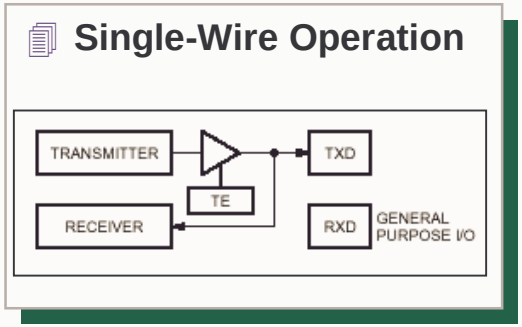


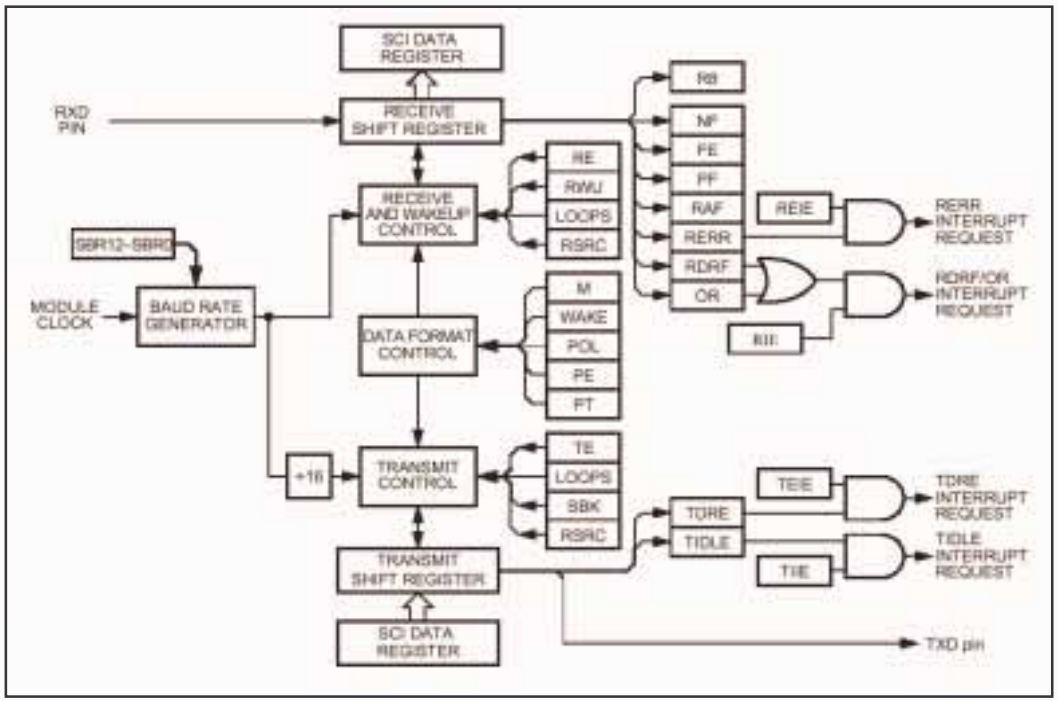
- ✓ Serial Peripheral Interface (SPI)
  - ✓ Supports LCD drivers, A/D subsystems, and MCU systems
  - ✓ Supports inter-processor communications in a multiple master system
  - ✓ Supports demand-driven master or slave devices with high data rates
- ✓ Serial Communications Interface (SCI)
  - ✓ Allows asynchronous serial communications with peripheral devices and other MCUs.
  - ✓ Full duplex serial port provides simultaneous data transmit and receive
  - ✓ Separately enabled transmitter and receiver
  - ✓ Can be configured for 8-bit or 9-bit data word lengths
- ✓ Synchronous Serial Interface (SSI)
  - ✓ On 56824
  - ✓ Details shown below

Serial Communication Interface

- Full duplex or single wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Separate receiver and transmitter CPU interrupt requests
- Programmable polarity for transmitter and receiver
- Two receiver wake-up methods: idle line or address mark
- Interrupt-driven operation with eight flags:
  - — Transmitter empty
  - — Transmitter idle
  - — Receiver full
  - — Receiver idle
  - — Receiver overrun
  - — Noise error
  - — Framing error
  - — Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection



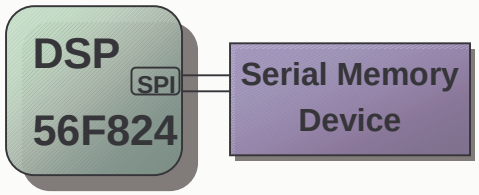


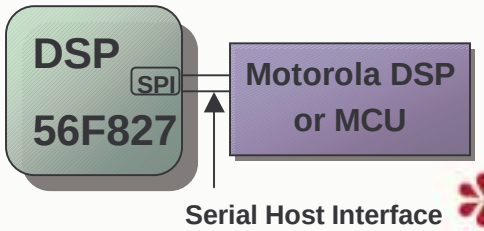


SPI: Serial Peripheral Interface

56F80x, 56824, 56F826/7:

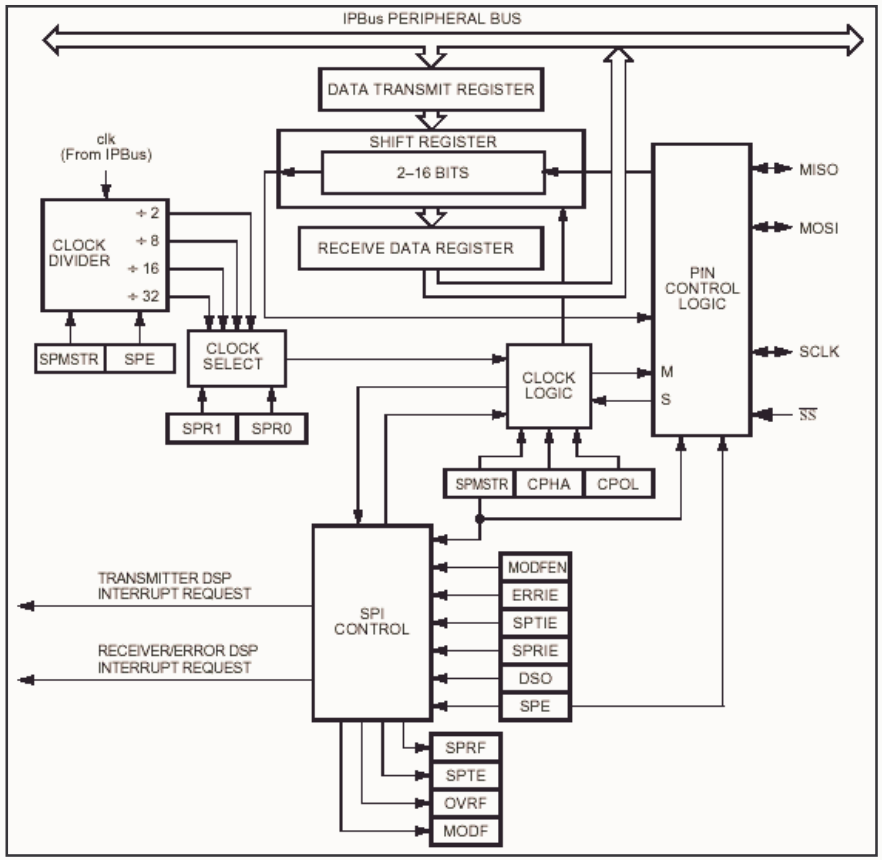
- ✓ **Full-Duplex Operation**
- ✓ **Master and Slave Modes**
- ✓ **Double-Buffered Operation With Separate Xmit and Rcv Registers**
- ✓ **Programmable Length Transmissions**
- ✓ **Programmable Transmit and Receive Shift Order**
- ✓ **Four Master Mode Frequencies**
- ✓ **Maximum Slave Mode Frequency = Bus Frequency**
- ✓ **Clock Ground for Reduced Radio Frequency (RF) Interference**
- ✓ **Serial Clock with Programmable Polarity and Phase**
- ✓ **Two Separately Enabled Interrupts for Receiver Full & Transmitter Empty**
- ✓ **Mode Fault and Overflow Error Flag With DSP Interrupt Capability**





Serial Peripheral Interface

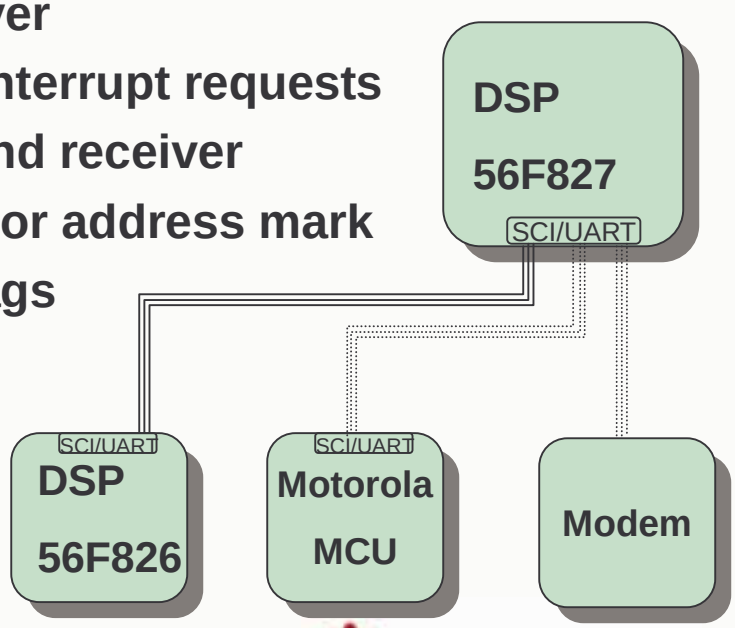
- Full-Duplex Operation
- Master and Slave Modes
- Double-Buffered Operation With Separate Transmit and Receive Registers
- Programmable Length Transmissions, 2 to 16 Bits
- Programmable Transmit and Receive Shift Order, MSB First or Last Bit Transmitted
- Four Master Mode Frequencies (Maximum = Bus Frequency ÷ 2)
- Maximum Slave Mode Frequency = Bus Frequency
- Clock Ground for Reduced Radio Frequency (RF) Interference
- Serial Clock with Programmable Polarity and Phase
- Two Separately Enabled Interrupts:
  - — SPRF (SPI Receiver Full)
  - — SPTE (SPI Transmitter Empty)
- Mode Fault Error Flag With DSP Interrupt Capability
- Overflow Error Flag with DSP Interrupt Capability



SCI: Serial Communications Interface

56F80x, 56F827:

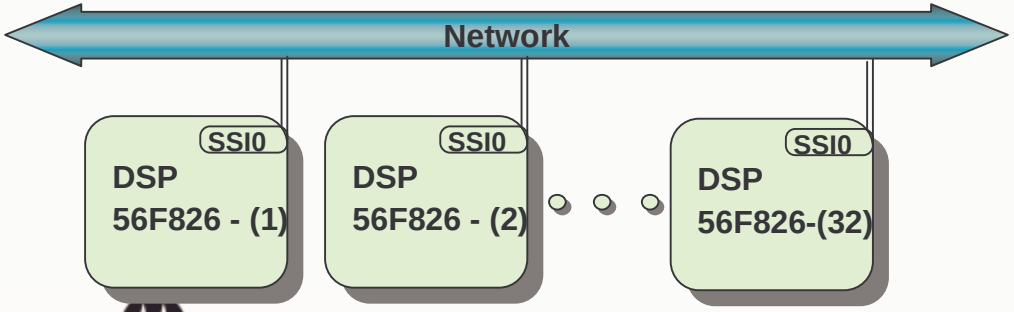
- ✓ **Asynchronous communications: UART**
- ✓ **Full duplex or single wire operation**
- ✓ **Standard mark/space non-return-to-zero (NRZ) format**
- ✓ **13-bit baud rate selection**
- ✓ **Programmable 8-bit or 9-bit data format**
- ✓ **Separately enable transmitter and receiver**
- ✓ **Separate receiver and transmitter CPU interrupt requests**
- ✓ **Programmable polarity for transmitter and receiver**
- ✓ **Two receiver wakeup methods: idle line or address mark**
- ✓ **Interrupt-driven operation with seven flags**
- ✓ **Receiver framing error detection**
- ✓ **Hardware parity checking**
- ✓ **1/16 bit-time noise detection**

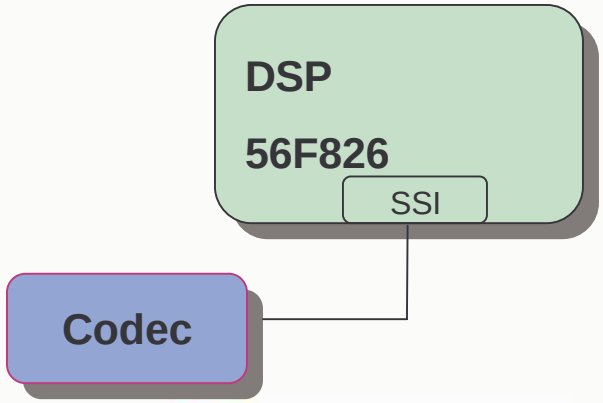


SSI: Synchronous Serial Interface

56824, 56F826/7:

- ✓ **Sophisticated programmable clocking**
  - ✓**Completely separate clock and frame sync selections for receive and transmit sections**
  - ✓**Independent or shared transmit and receive**
  - ✓**Normal mode operation using frame sync**
  - ✓**Gated Clock mode operation requiring no frame sync**
  - ✓**Programmable internal clock divider**
  - ✓**Program options for frame sync and clock generation**
- ✓ **Programmable word length (8,10,12, or 16 bits)**
- ✓ **SSI power-down feature**
- ✓ **Network Mode**





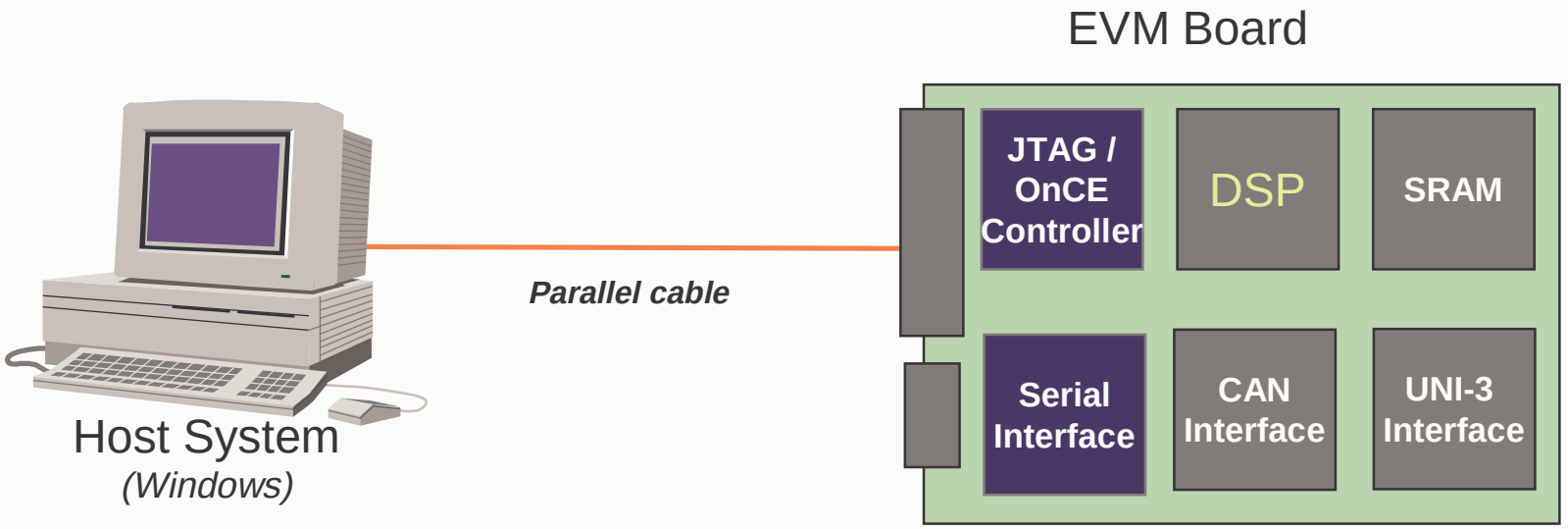
DSP56800/800E Evaluation Module (EVM)

DSP Evaluation Module (EVM) Kit

The EVM kit includes the everything required to start developing code immediately. It includes all documentation, required cabling, power supply, CodeWarrior IDE, and Embedded software development kit (SDK).

Standard Features:

- ✓ Parallel port Connection to Host PC
- ✓ Non intrusive debug via OnCE port
- ✓ JTAG Connector
- ✓ Expansion Memory (not on 801)
- ✓ Standard UNI-3 connection (2 on 805/7)
- ✓ Motion Control Circuitry
- ✓ CAN PHY layer (not on 801)
- ✓ Universal Power Supply
- ✓ Code Warrior CD w/60 day evaluation license
- ✓ Embedded SDK w/permanent license



The Software Development Kit (SDK) An Advanced Software Infrastructure

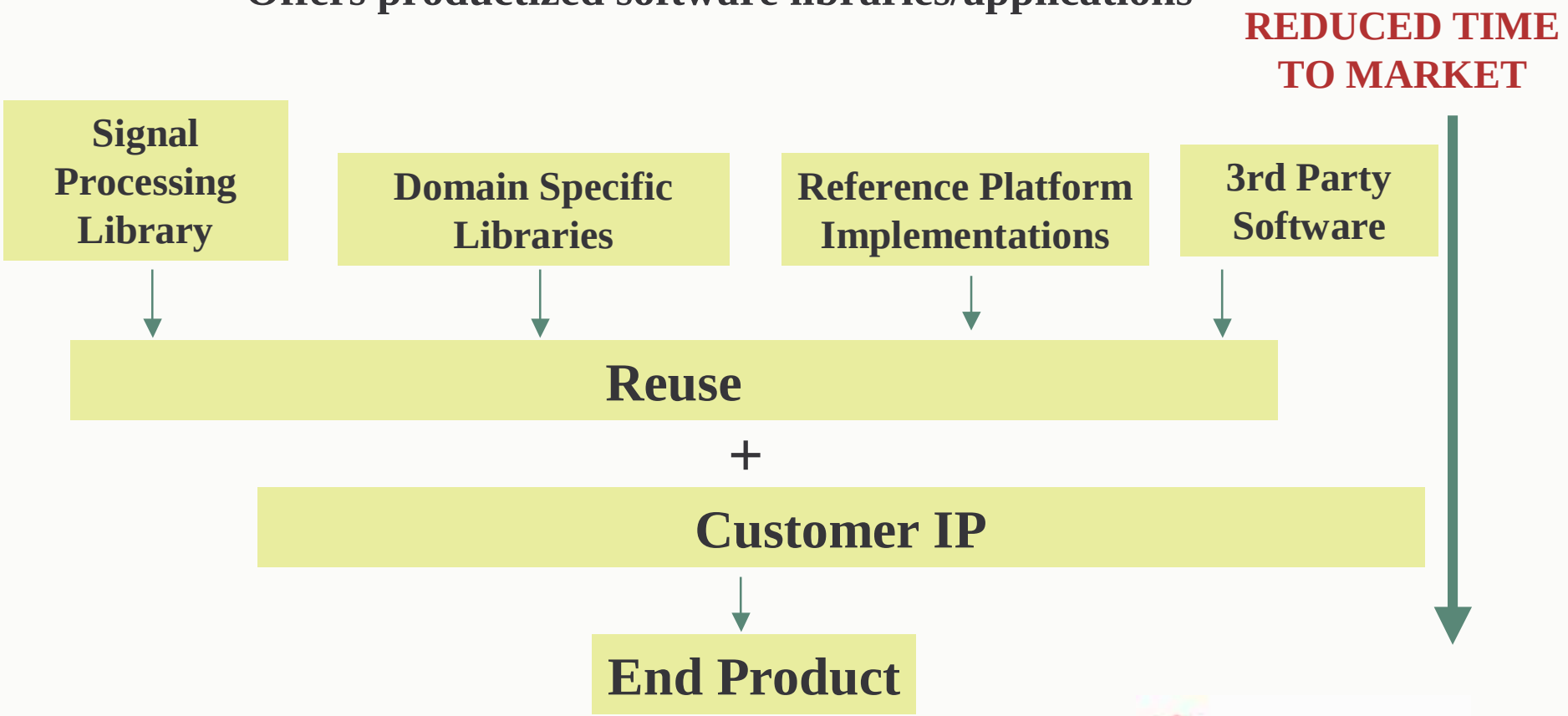
The SDK or Software Development Kit offers more than just a set of Signal Processing Libraries.

The SDK is a modular, integrated, high-performance real-time software infrastructure designed specifically for embedded processors. The infrastructure allows the customer to quickly add their unique IP (intellectual property) to the software solution with a minimal resource investment .

The benefit is a low risk, seamless transition for software applications across multiple hardware platforms which enhances the customer's time to market.

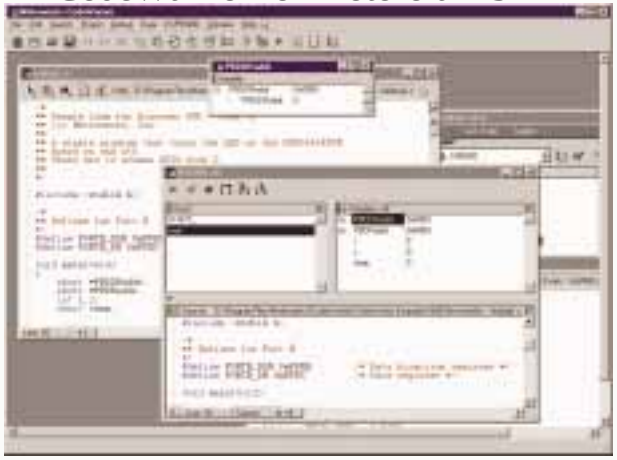
The SDK Differentiation

- **API environment within a SDK framework**
- **Provides domain specific value added capabilities**
- **Offers productized software libraries/applications**



DSP56800/800E Development Tools

CodeWarrior for Motorola DSP



PC Master: Motion Control Visual Analysis

- ✓ **Award Winning CodeWarrior IDE**
- ✓ **Language & Context Sensitive Editing**
- ✓ **Graphical Drag & Drop Project Management**
- ✓ **Graphical Source and Assembly debugger**
- ✓ **Optimizing C compiler (Global and DSP specific)**
- ✓ **Open Plugin Architecture**

Rapid Software Development
Maximized Productivity of
Software Resources

- ✓ **Real Time Data Capture**
- ✓ **Real Time Data Logging**
- ✓ **Graphical data Visualization**
- ✓ **Command and Status exchange**
- ✓ **Real time graphical motion analysis**
- ✓ **Safe for use in full power operational systems**

Metrowerks CodeWarrior

- **Superior Editor**
  - **Custom Key Words and key bindings**
  - **Pull down list for functions and headers**
  - **Drag and drop editing**
- **Flexible Project Management**
  - **User defined file mappings**
  - **Drag and drop file management**
  - **Stationery (starting templates)**
- **Unique Graphical File Compare**
  - **Graphical display**
  - **Apply differences from file to file**

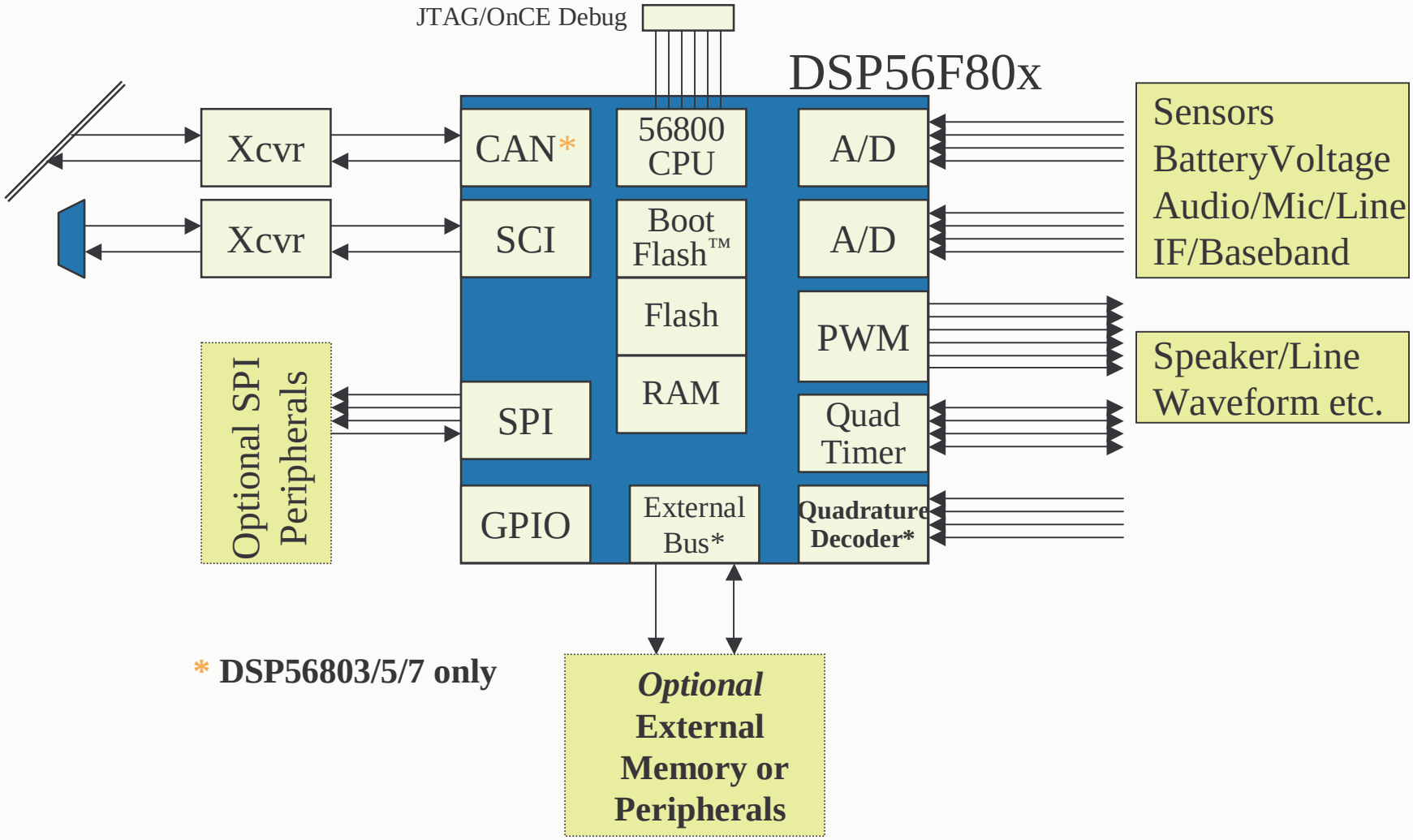
Metrowerks CodeWarrior

- **State of the Art Search Engine**
  - **Controllable file search order**
  - **Save and re-use user defined set of files**
  - **Search user defined set of files**
  - **Batch all instances**
- **Advanced Browser**
  - **Browser catalog of symbols**
  - **Complete code navigation**
  - **Available from any source window**
- **Extensive Desktop Version Complement**
  - **Desktop Prototyping, Debugging, Interface design**
  - **200,000 CodeWarrior Users World-wide**
  - **Mac, Windows, Solaris, Java, Linux**

Target Markets

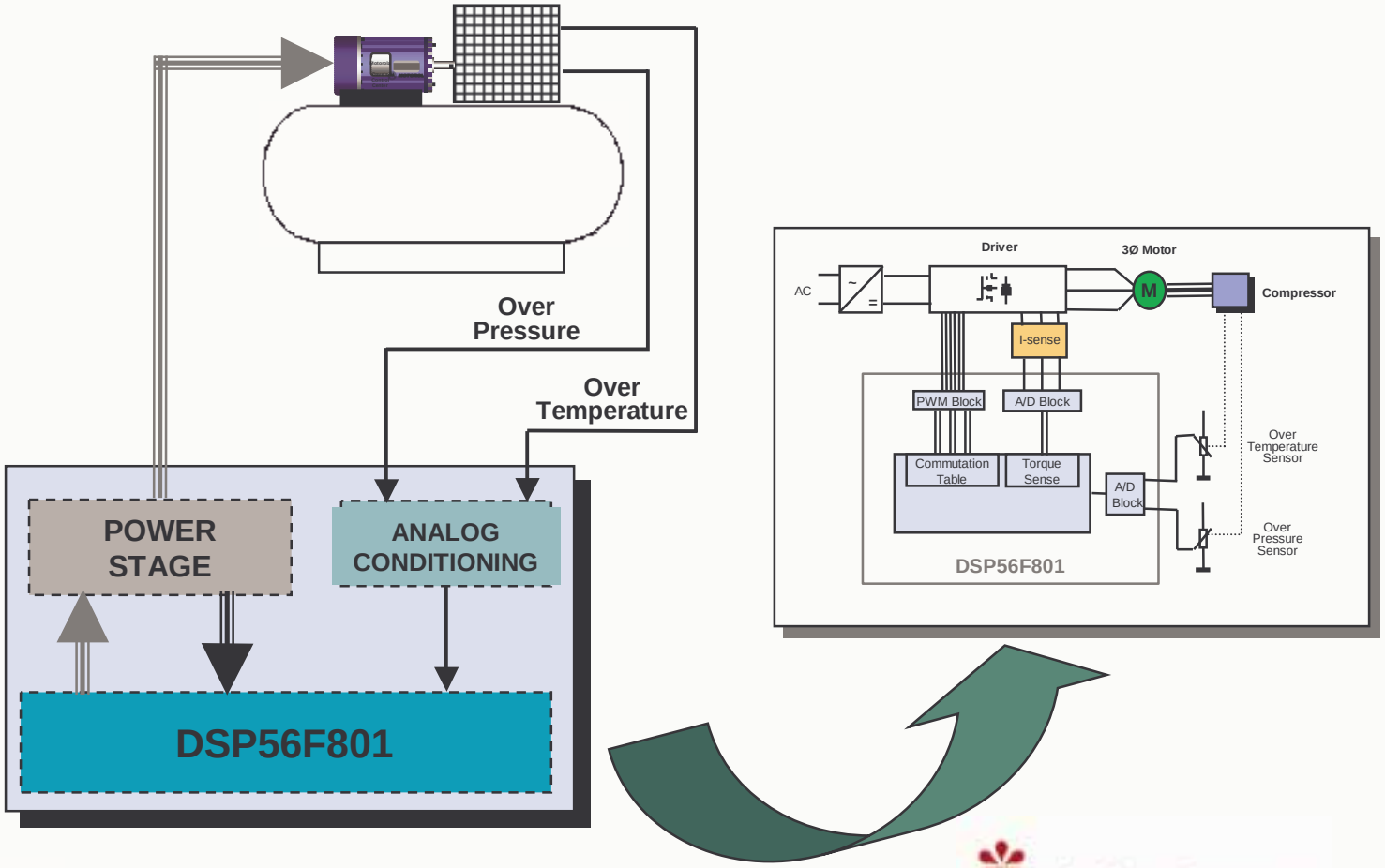
- Network/Client Devices/VoIP
- Telephony
- Consumer Audio
- Transportation
- Industrial
- Office/Home Automation
- Medical
- Home Appliances
- HVAC

General Embedded Application



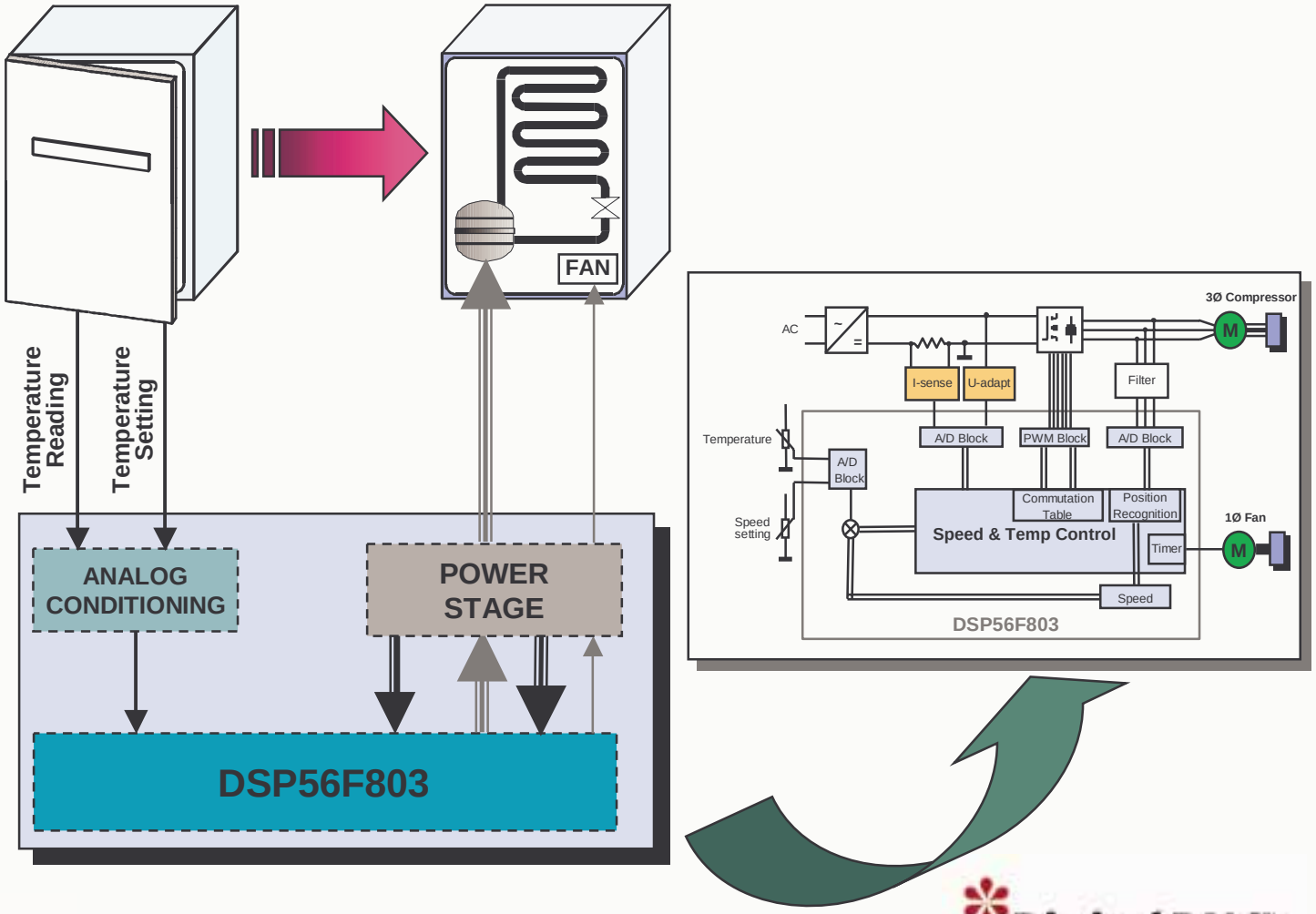
Industrial Compressor Drive

Direct-Drive, 3-Phase, AC Induction Motor
Using Direct Torque Control
w/ Over Temperature & Over Pressure Sensing



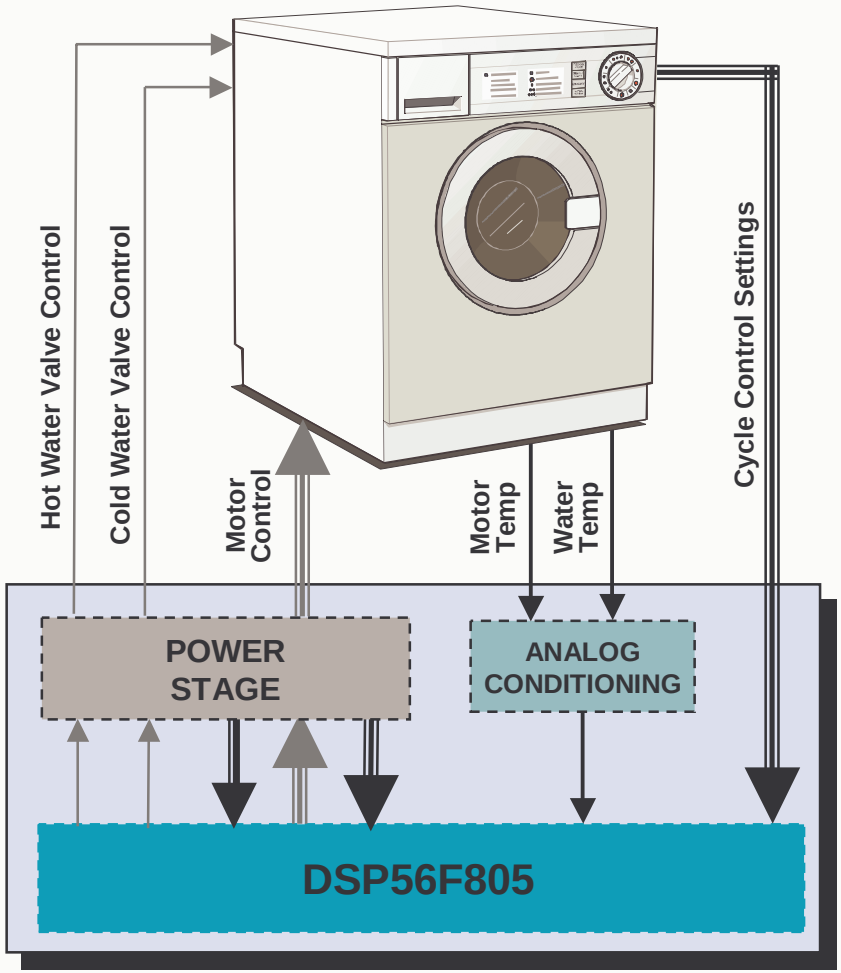
Refrigerator Compressor Drive

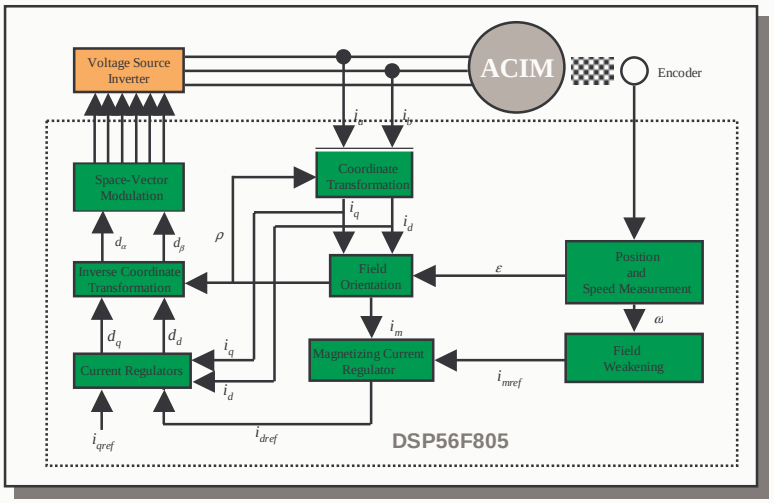
3-Phase, Sensorless BLDC Motor
Using Speed & Temperature Regulation Control



Washing Machine

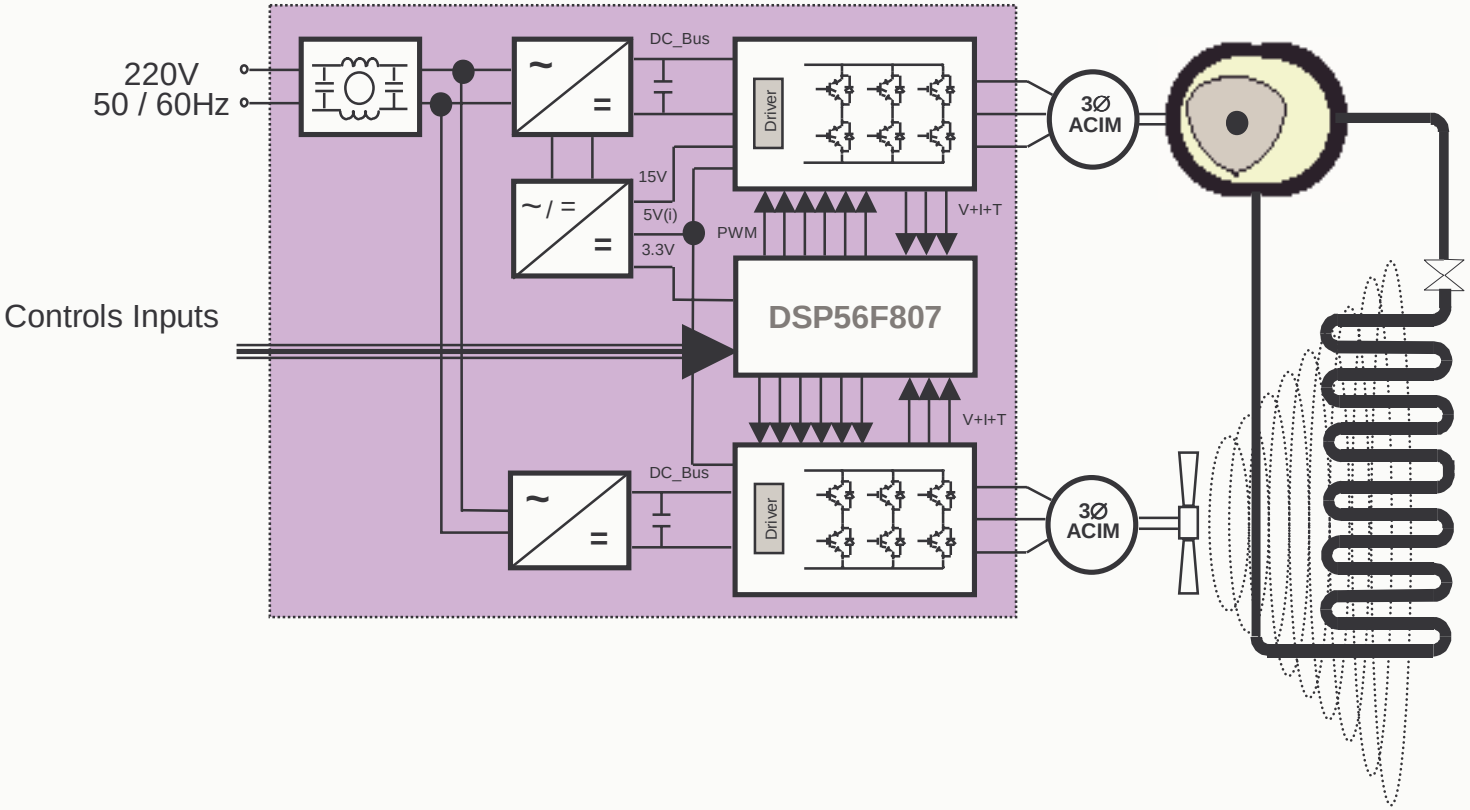
Indirect Drive, 3-Phase, AC Induction Motor Using Vector Control





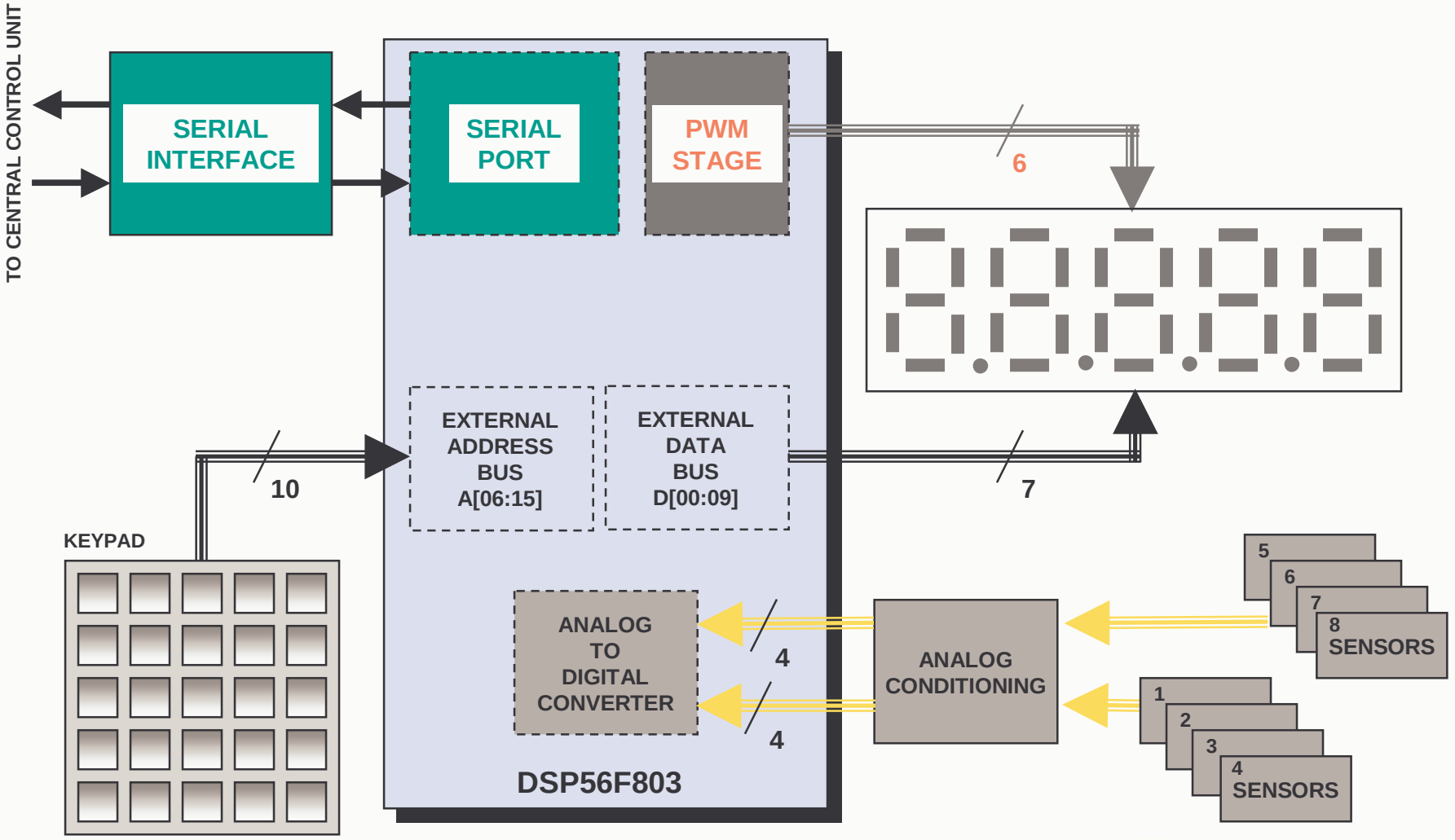
Air Conditioning System

Two, 3-Phase AC Induction Motors Using Vector Control



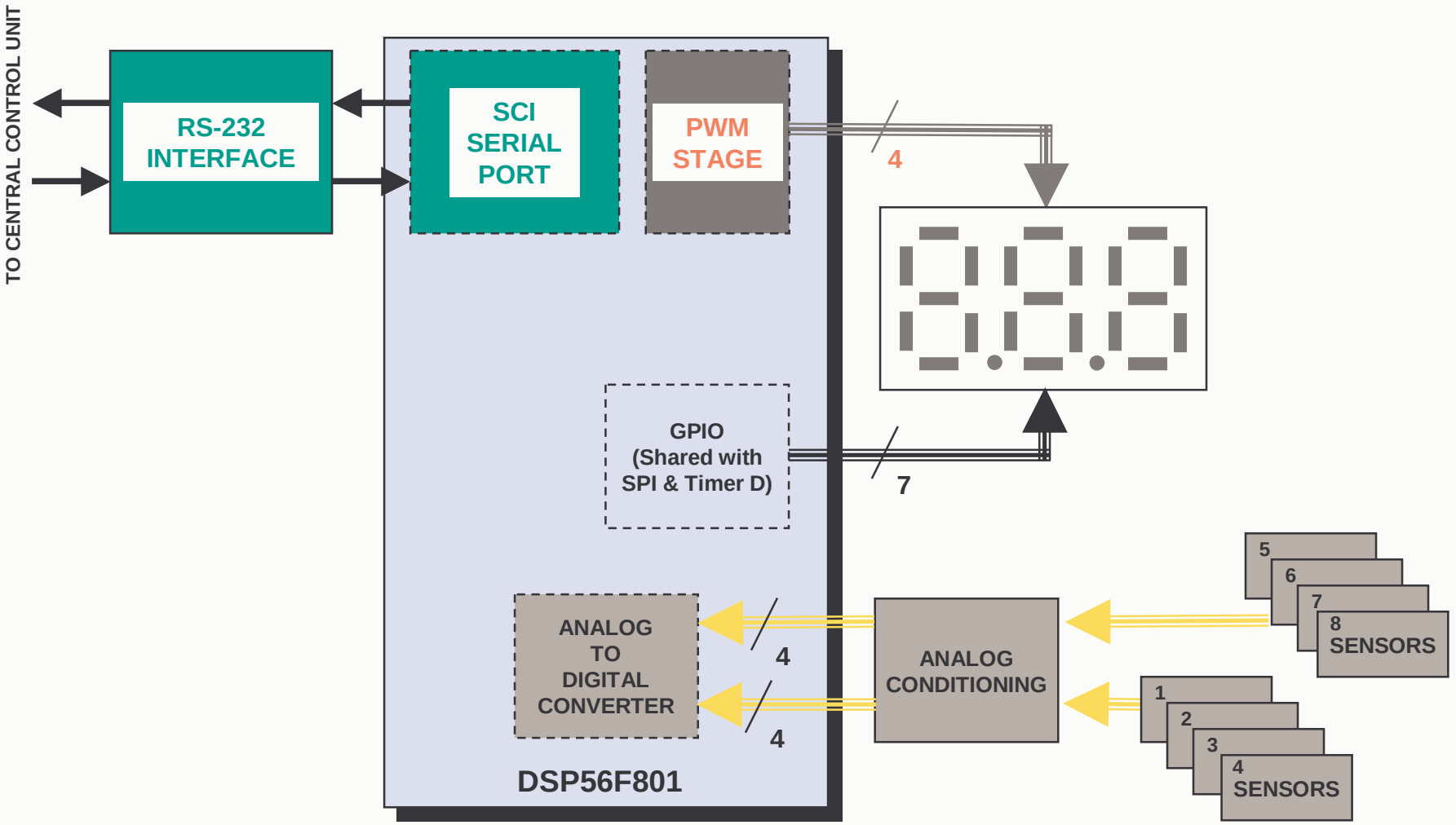
Remote Monitoring System

With Local Readout and Control Inputs Using **DSP56F803**



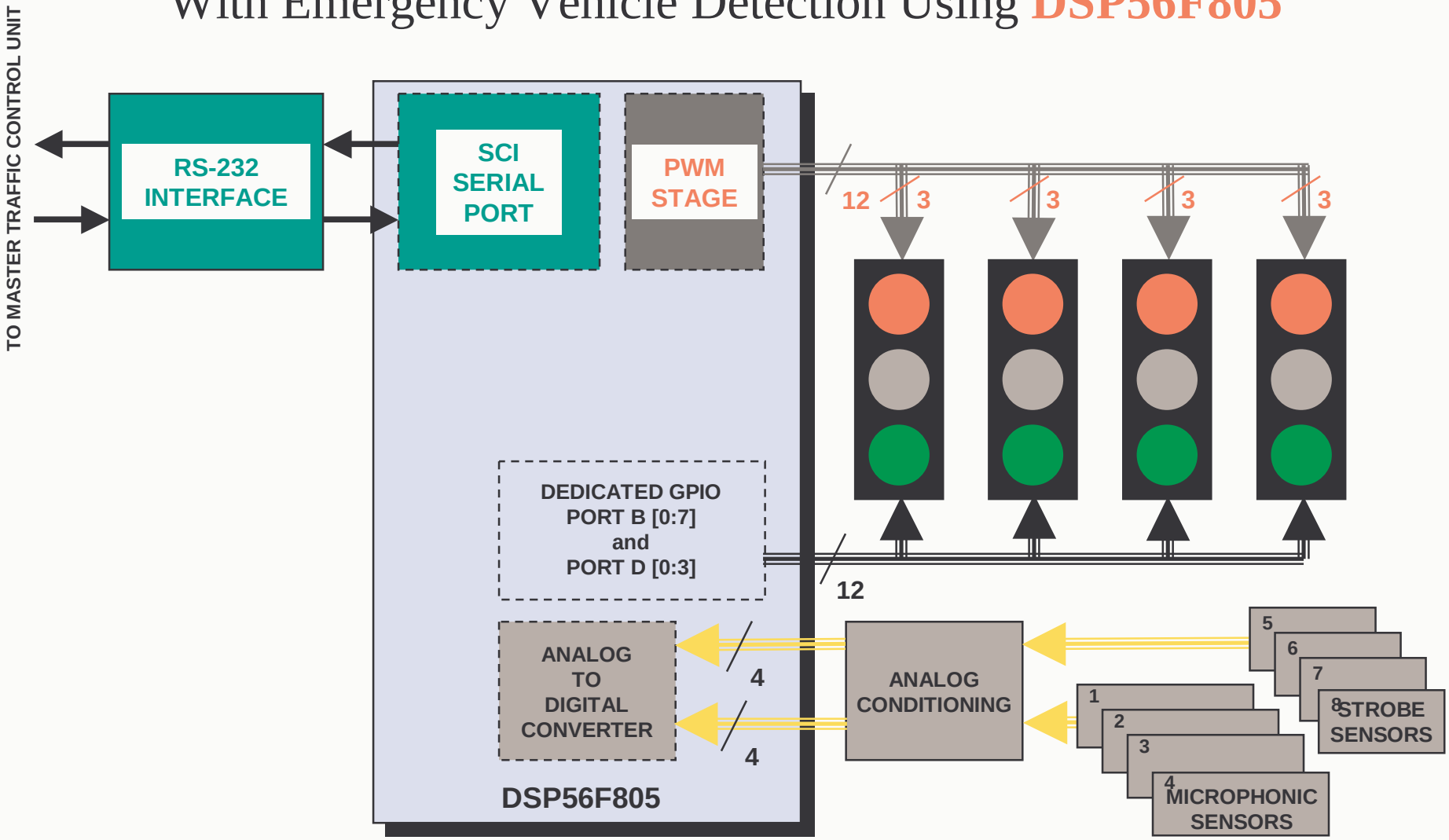
Remote Monitoring System

With Local Readout Only Using **DSP56F801**



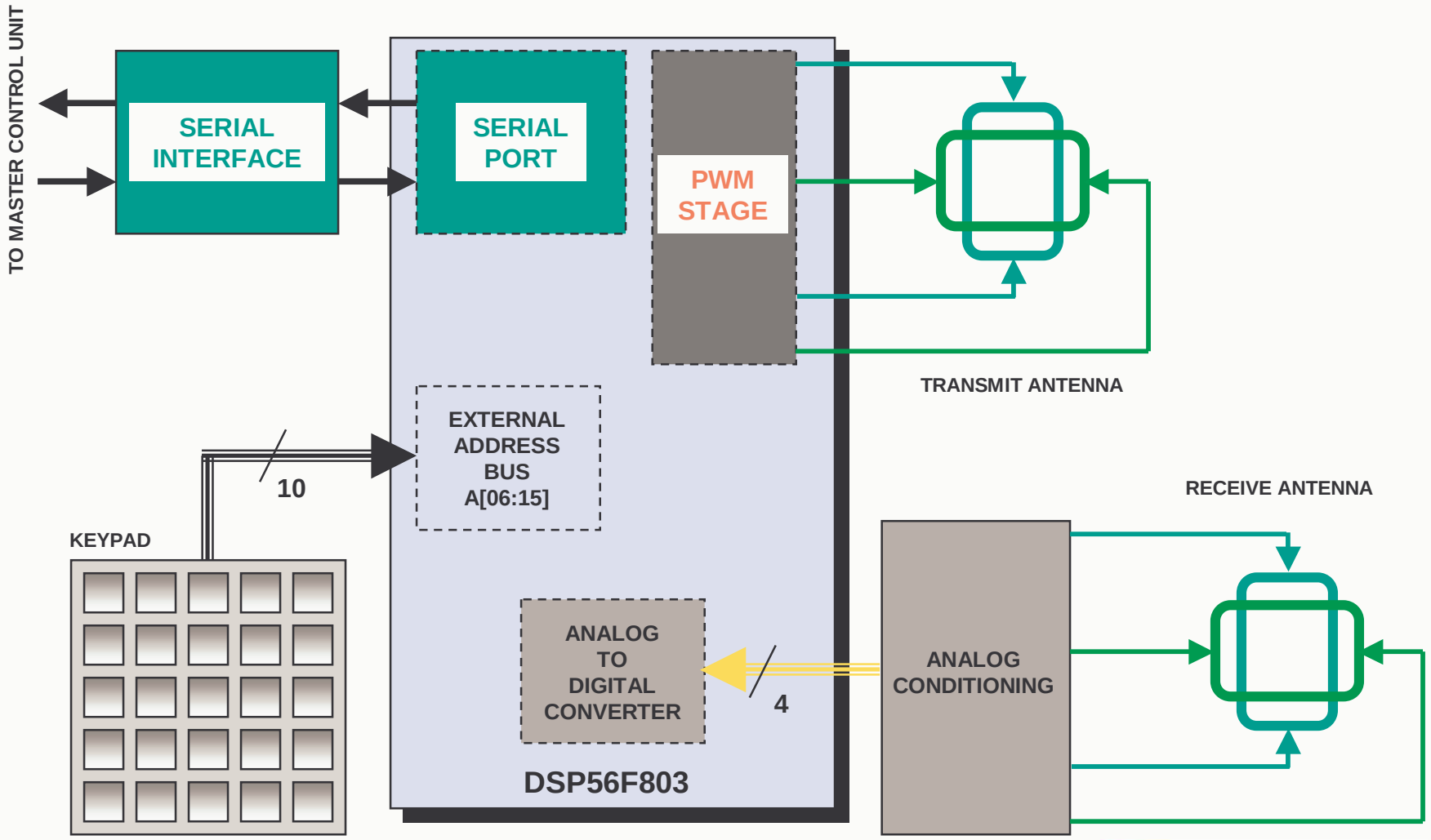
4-Way Traffic Light Control System

With Emergency Vehicle Detection Using DSP56F805



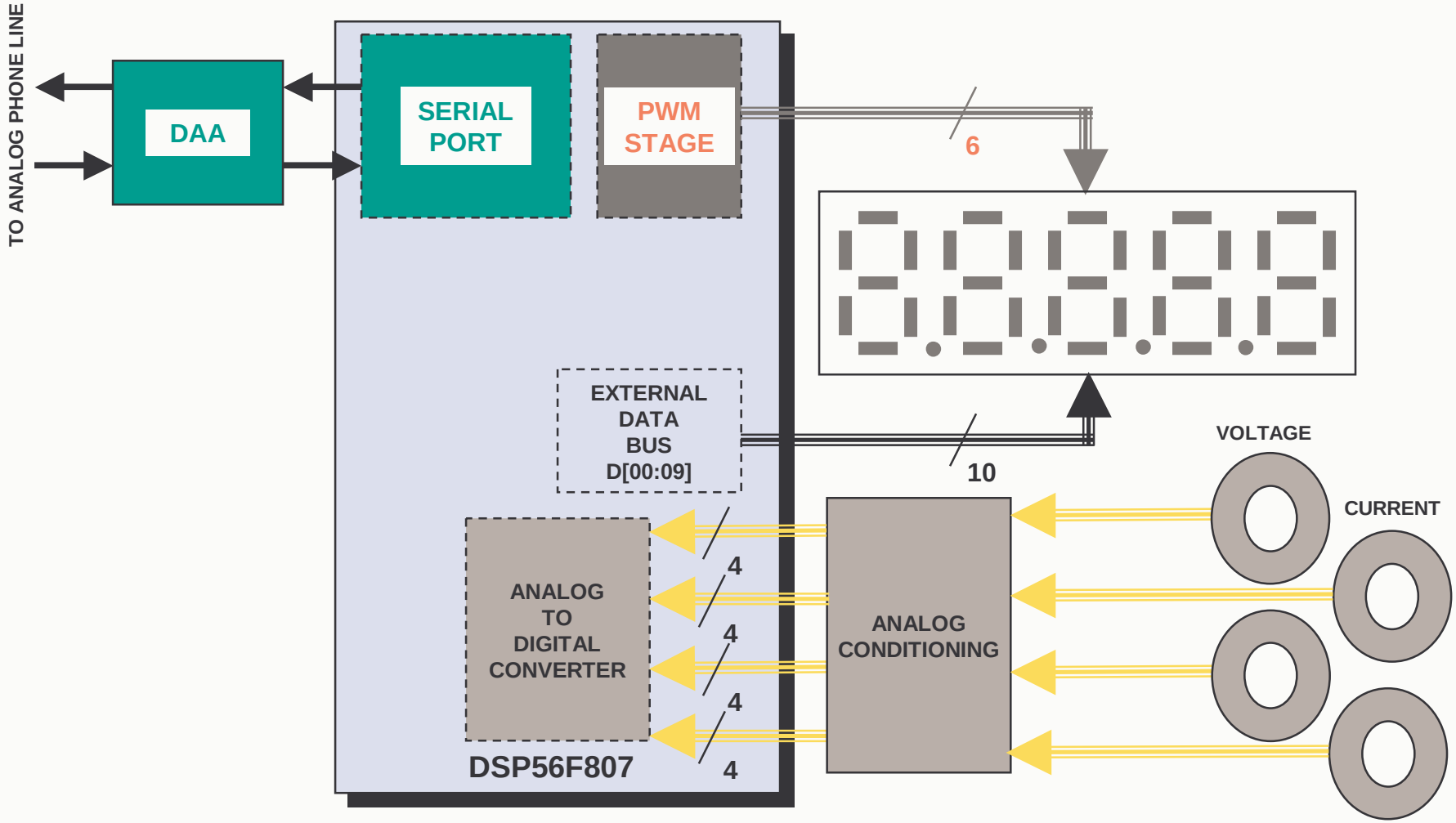
Tag Reader System

With Control Inputs Using **DSP56F803**



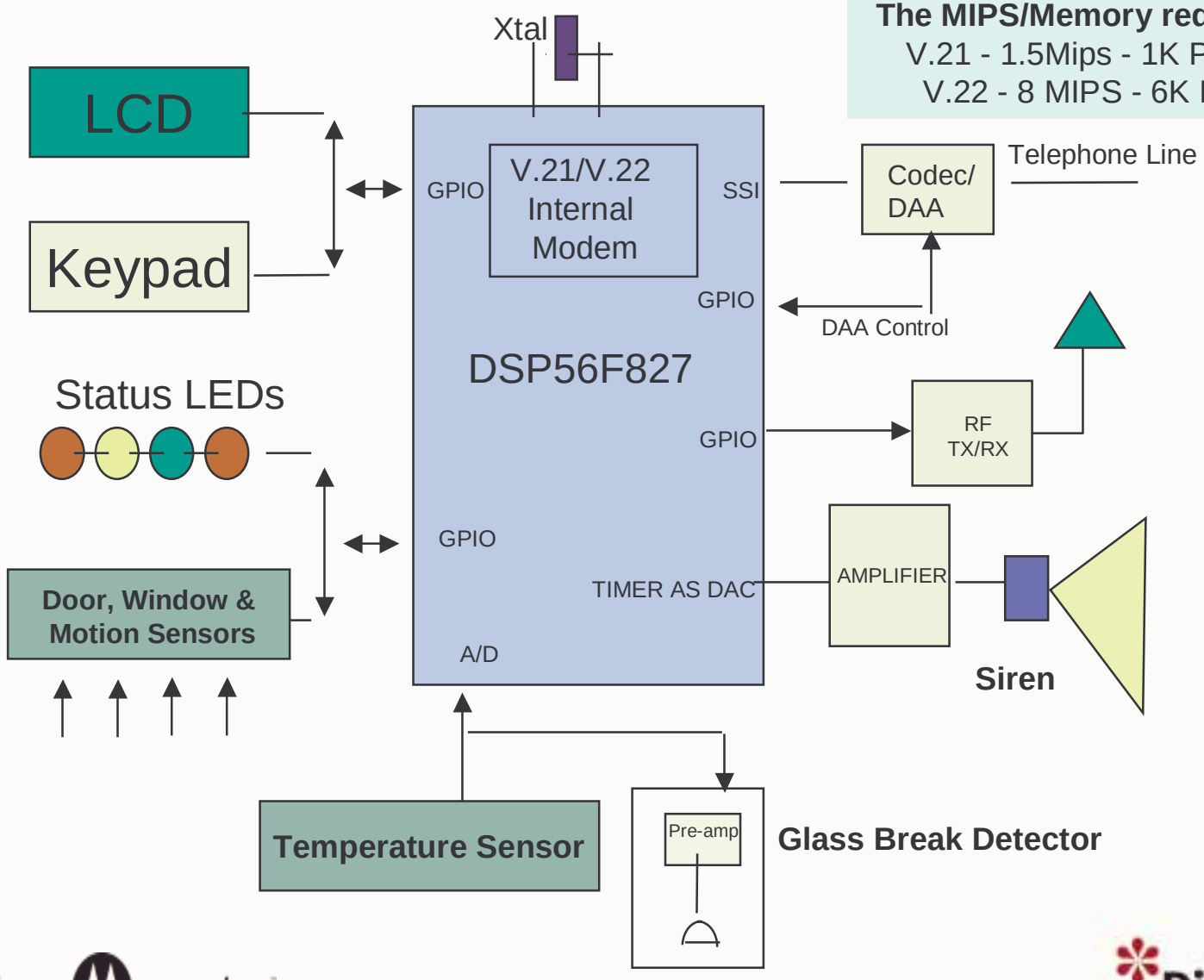
Automatic Meter Reader (AMR) System

3-Phase Unit With Local Readout Using **DSP56F807**



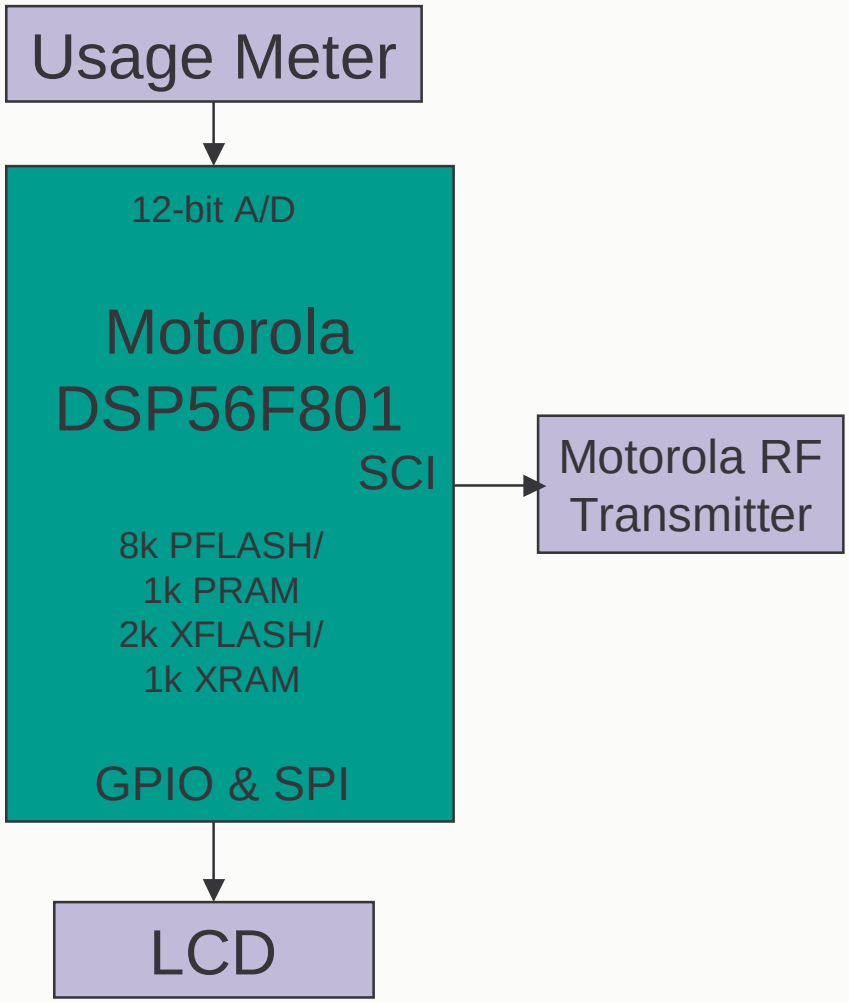
DSP56F827: Monitored Home Security Application with Modem

The MIPS/Memory required for a modem:
V.21 - 1.5Mips - 1K Program, 1.5K Data
V.22 - 8 MIPS - 6K Program, 2K Data



Utility Meter

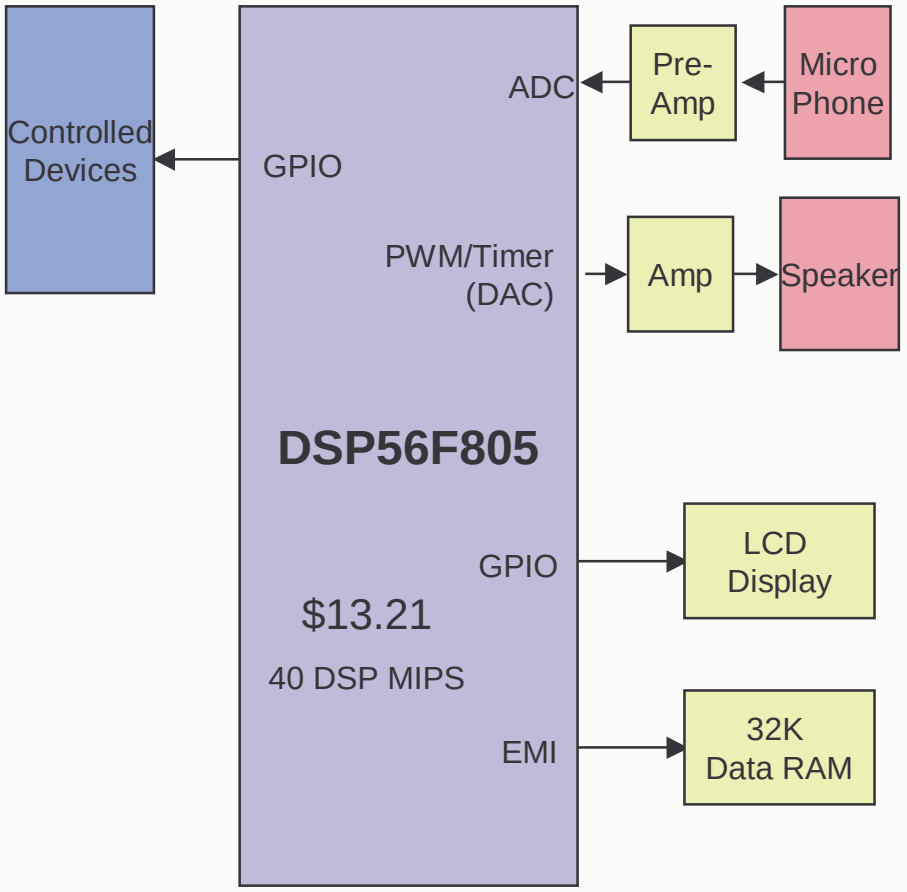
‘801: 40 DSP MIPS at 40 MHz



Voice Enabled Controller

Hands-Free Speech Recognition System

Motorola F805



DSP56800/800E Development Tools

- Embedded Software Development Kit (SDK)
  - Website: http://www.motorola.com/sps for free copy
- Metrowerks Codewarrior Integrated Development Environment (IDE)
  - Linker/Assembler/C Compiler/Debugger/Core Simulator
  - Ordering Numbers: CWDSP56800 & CWDSP56800E
  - Free 30 day evaluation license with every EVM
  - Contacts:
    - Metrowerks Website: http://www.metrowerks.com
    - Technical Support: http://www.metrowerks.com/support/contact
    - Codewarrior U Website: http://www.CodewarriorU.com

Motorola DSP Accessing Information

- Motorola Semiconductors Website
  - http://www.motorola.com/sps
- Technical Support
  - http://e-www.motorola.com/support/index.html
- Technical Helpline
  - http://e-www.motorola.com/webapp/RUHP.jsp
- Local Distributor Branch Product Managers